Solartron
1210/RVC 500

MP MASTER
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1210/RVC 500
RANDOM VIBRATION CONTROLLER

MAINTENANCE MANUAL

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RVC MAINTENANCE MANUAL

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CHAPTER 1

USING THE RVC MAINTENANCE MANUAL

The information contained in the RVC maintenance manual provides for fault diagnosis, fault rectification and calibration of the RVC, both on site and at a service centre. **See safety notes overleaf.**

On site servicing is normally restricted to board replacement. To aid in the location of a faulty board the RVC has an in-built diagnostic program. The selection of this is described in the RVC operating manual, whilst the interpretation of the diagnostic information that the program presents on the RVC display is described in Chapter 2 of the maintenance manual.

When a fault does not permit the in-built diagnostic program to operate then the 'system build procedure' may be used. This is described in Chapter 3. The procedure provides for the gradual build up of the RVC from the basic mainframe to a fully operational system, with each fault being corrected by the service engineer as it is detected.

Analogue calibration is described in Chapter 4. Apart from the clock frequency adjustment on board 51, analogue calibration is done only on the input and generator sections of board 52. If this board is found to be faulty on site it is recommended that the RVC is re-calibrated once the serviceable board 52 is fitted. This will normally mean sending the instrument back to a service centre, unless, of course, the required test gear is available on site. In an emergency a pre-calibrated board 52 can be fitted as a temporary measure, but the accuracy of the affected instrument can not be guaranteed and re-calibration of board 52 in the instrument should be done as soon as possible.

Chapter 5 contains the RVC check procedure, which should be used following fault rectification and/or recalibration.

When fault finding, at either board or component level, it is advisable to have a basic understanding of the way in which the RVC hardware operates. This can be obtained by reading the following chapters in the maintenance manual:

Chapter 6, 'System Description'. This chapter describes the data flow between the various RVC 'modules'. The module 'breakdown' of the RVC system is shown in block diagram form in Chapter 6.

Chapter 7, 'RVC Bus Operation'. This chapter describes the RVC 'master-slave' relations, bus priority, program interrupts and the bus 'read' and 'write' cycles.

Chapter 8, 'Module Descriptions'. This chapter contains the module-related sections that give the technical information peculiar to individual RVC modules.

Chapter 9, 'CRT Replacement', contains all the information necessary to replace a faulty CRT with a serviceable one.

Chapter 10 contains pcb related sets of component parts lists and circuit diagrams, in numerical order of pcb.

See safety notes overleaf.

SAFETY

Extreme care should be used when working on the interior of the RVC while this instrument is, or has recently been, switched on. Hazardous voltages exist in the area of the ac supply circuitry and the CRT display. To ensure a safe working environment, it is recommended that you adhere strictly to the following precautions:

* Ensure that your feet are always fully insulated from the floor, either by standing on a rubber mat or by wearing rubber boots.

* Always use insulated handle tools, of the correct voltage rating.

* Always use the 'single hand' technique, i.e. work with only one hand in the harzardous voltage area. Keep the other hand away from earthed surfaces, such as the RVC mainframe.

If the RVC has recently been switched off it is advisable to discharge any capacitors in hazardous voltage areas with a resistor of suitable value; or, allow the capacitors time to discharge through the RVC internal circuitry.

With regard to a possible implosion of the CRT, great care should be used when manipulating the components around the fragile glass neck. Protective eye goggles or spectacles with side shields should be worn at all times. As a further precaution, a protective apron should be worn.

CHAPTER 2

RVC SELF DIAGNOSIS

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CHAPTER 2 RVC SELF DIAGNOSIS

2.1 INTRODUCTION

To check the correct operation of the digital circuitry, and to locate a possible fault, the RVC is able to perform a power up test and a system check. With these diagnostic programs, faults can be diagnosed down to board level or, in some cases, component level. For the programs to function, certain areas must be fully operational; in particular, board 1, the system controller (with the exception of the 'scratch pad' RAM).

The power-up test is executed as part of the system initialisation procedure (when the system software is entered via the LOAD vector). This occurs when:

* the ac supply (mains) is switched on

* a 'watchdog' reset instruction is executed

* the SBUG command 'X7000' is given.

The areas covered by the power-up test are:

1. The display, including the full bit store, data buffer, command buffer and cursor RAM.

2. The 'scratch pad' RAM on the system controller (board 1).

3. The instruction store (board 28) of the system controller

4. The data store (board 4)

5. The array processor (boards 8, 9 x 2, and 10)

6. The DFT logic of the array processor

7. The test store.

The system check is started by the user, either by pressing the SYSTEM CHECK soft key in the SELF TEST menu or by giving an equivalent GPIB command. The check comprises the power-up test described above, plus a test on each of the following areas:

8. the GPIB interface (boards 5, 6 and 7)

9. the plotter interface (board 11)

10. the keyboard interface (board 53) and the front panel keys.

The power up test, also, can be started by the user, either by pressing the POWER UP TEST soft key in the SELF TEST menu or, again, by giving the equivalent GPIB command.

The power-up test may be disabled for diagnostic purposes by setting switch S1/3 to 'ON' on board 1. This action does not disable the system check.

Details of each test done in the power up test and the system check are given in Section 2.3.

2.2 TEST SEQUENCE

After a test program has been requested, but before the tests start, the system software executes an initialisation cycle. This resets all the hardware, with the exception of the battery sustained Test Store, and initialises the RVC control program. On the successful completion of the initialisation cycle, a 'bleep' signal is output from the RVC. This signal indicates that the system controller (board 1) is operational. When the tests begin, the message 'POWER UP TEST' is displayed. If the message does not appear then a fault on the display interface should be suspected.

Each test is allocated a line of text on the display. This line contains the test title, the test result and, in the case of a test failure, the fault data. Each line appears as soon as the relevant test is completed. If a test is successful a PASSED result is indicated and the next test begins automatically. In the case of a completely successful power up test no user action is necessary and the RVC automatically enters it's initial working state. A completely successful system check is almost the same, but with this the initial working stage of the RVC is not entered until the ENTER key is pressed on the numeric keypad. This allows the user to check the keyboard (test 10). A display resulting from a successful system check is shown in Fig. 2.1.

```
                              POWER UP TEST     SYSTEM   S/W ISSUE XG

 1. DISPLAY                        PASSED       DISPLAY  S/W ISSUE XD
 2. SCRATCH RAM                    PASSED
 3. CHECK SUM                      PASSED
 4. DATA RAM                       PASSED
 5. ARRAY PROC                     PASSED       ARRAY P. S/W ISSUE XB
 6. DFT PROC                       PASSED
 7. TEST STORE                     PASSED

                              SYSTEM CHECK

 8. GPIB                           PASSED
 9. PLOTTER                        PASSED
10. KEYBOARD     PRESS A KEY        OP)        PRESS ENTER TO FINISH
```

Fig. 2.1 System check display

Note that the display also indicates the status and issue of the software fitted to the controller (board 28), display (board 3) and array processor (board 8).

If a test is failed, execution of the diagnostic program is halted and against the FAILED legend for that particular test the user prompt message 'PRESS ANY KEY TO CONTINUE' is displayed. Any key on the main keyboard can be used for this purpose, except 'rtl', SELF TEST, or those keys on the numeric keypad. When testing is continued the prompt message is cleared. A fault may be located by means of the fault data, whose significance is explained in Section 2.3. If several faults occur on the same test, pressing a front panel key to continue simply steps the diagnostic program from fault to fault until the test is completed.

A test sequence may be aborted, either by selecting shift/SELF TEST or by giving the GPIB command 'TQ?'. If it is capable of doing so the RVC then enters its initial working state.

On test completion the user is reminded of any fault that may have occurred, by the message 'SYSTEM TEST FAILURE'. This appears in the top left hand corner of the display.

2.3 TEST DETAILS

For each test the fault data consists of three four-digit hexadecimal numbers:

'AAAA' 'BBBB' 'CCCC'

The first number, 'AAAA', is either a failure address or an error number. The second number, 'BBBB', is the value which the diagnostic program expects as the test result, i.e. the 'expected' value. The third number, 'CCCC', the value obtained that caused the fault, i.e. the 'obtained' value.

Test 1 DISPLAY

Test 1 individually tests each location in the display buffer memory (board 3).

Error Interpretation

Test status display:

1 DISPLAY A (or B) AAAA BBBB CCCC FAILED PRESS ANY KEY TO CONTINUE.

AAAA: address of failed location.

BBBB: expected value.

CCCC: obtained value.

Address	ICs															
	msb															lsb
8000-BFFE	IC50	36	22	9	51	37	23	10	52	38	24	11	53	39	25	12
								Bd 2								
	Hi byte				Lo byte											
C000-C7FE	IC21				IC32											
C800-CFFE	IC20				IC31											
	Bd 3				Bd 3											
D000-D7FE	not used				IC30/Bd 2											

Fig. 2.2 Display RAM ICs

Using the above information and Fig 2.2 allows the faulty IC to be identified.

Note: Display A or Display B refers to the two halves of the full bit store, i.e. foreground and background.

Test 2 SCRATCH RAM

Test 2 makes an individual test of each location of the scratch pad RAM located on board 1. This is done non-destructively and verifies that all bits in each word can be set and cleared.

The 16 word workspace used by this test is not tested.

Error Interpretation

Test status display:

2 SCRATCH RAM AAAA BBBB CCCC FAILED

AAAA: address of failed location (0- 17FE even only).

The address ranges shown below test the RAM IC's (all on board 1), which are pertinent to the most significant byte and the least significant byte as indicated.

Address Ranges	Most Significant Byte	Least Significant Byte
0-7FE	IC59	IC58
800-FFE	IC43	IC42
1000-17FE	IC9	IC7

BBBB: expected value

CCCC: obtained value

Test 3 CHECKSUM

Test 3 calculates and checks the checksum of each individual PROM on board 28. The valid checksums are stored in IC11 and IC12 (the PROMS containing the test programs), and these IC's are not tested.

Error Interpretation

Test status display:

3 CHECKSUM AAAA BBBB CCCC FAILED

AAAA: identity of failed IC, in hexadecimal. IC numbers range from 1 (IC1) to 18 (IC24).

BBBB: expected checksum, which should correspond to the checksum written on the PROM.

CCCC: obtained checksum.

Test 4 DATA RAM

Test 4 tests the main machine data storage RAM (Board 4) and is also a good RVC bus exerciser. It is a destructive test which starts by writing to each location using the location address as data. The memory is then scanned again. The data is checked against its address, inverted and checked again.

Error Interpretation

Test status display:

4 DATA RAM AAAA BBBB CCCC FAILED

AAAA: address of failed RAM (0 - BFFF even and odd).

BBBB: expected value. This will be the equal or the inverse of the address (AAAA).

CCCC: obtained value.

Using the above information, and Fig. 2.3, allows the faulty IC to be identified.

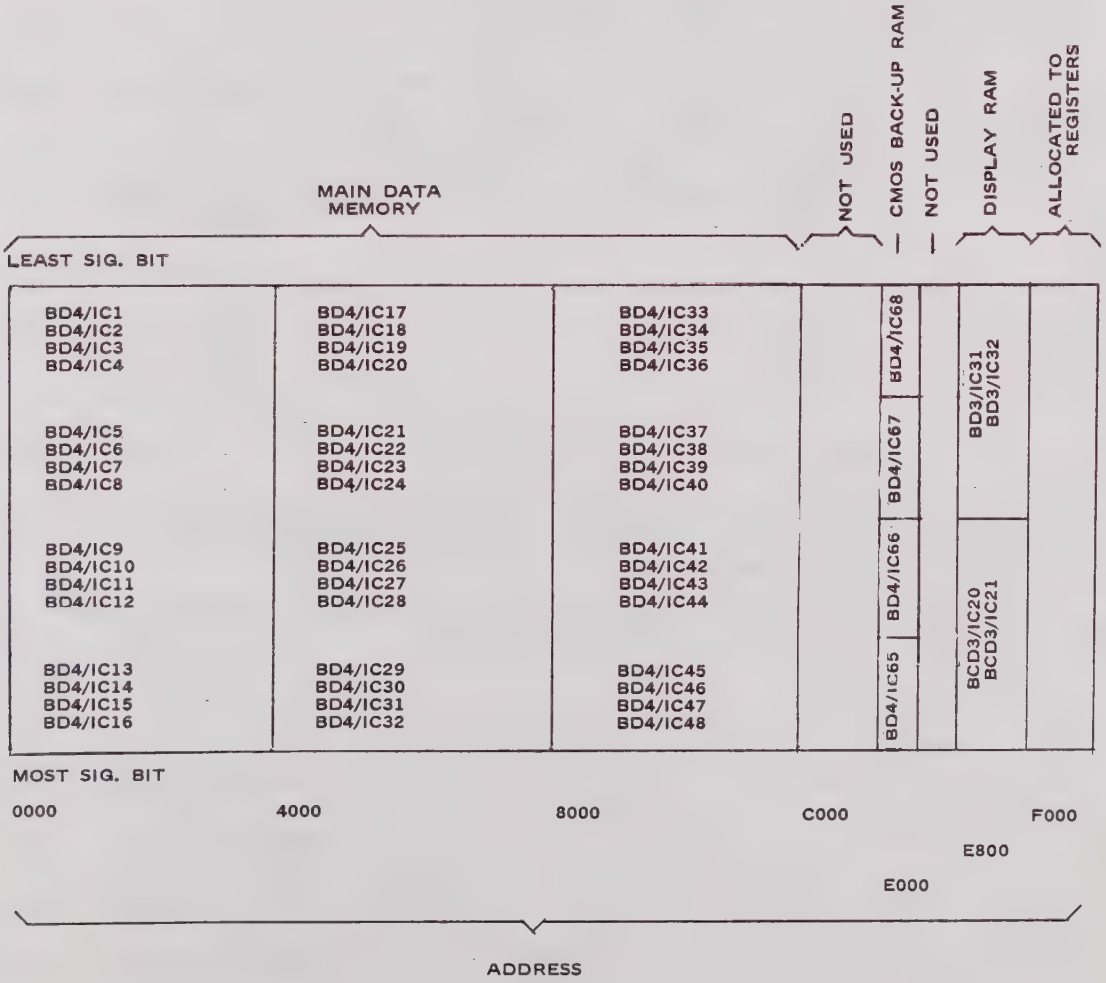

Fig. 2.3 1200 Bus Address Space Allocation

Test 5 ARRAY PROCESSOR

The array processor is the main arithmetic processing unit within the RVC. Test 5 verifies the major control and data input/output hardware of this module.

The control board, both ALU boards, and the multiplier board, all contribute to the correct result from this test. The operand memory of the array processor is also verified. The test executes a DMA input and output of known data from the RVC memory (Board 4) and then checks that the output data are correct.

Error Interpretation

Test status display:

5 ARRAY PROC AAAA BBBB CCCC FAILED

AAAA: address of a location containing an incorrect value. This address can range from 0 to 1FFF (0 to 8,191 dec.) to include the 8k words of storage within the operand memory. The operand memory comprises two storage areas, one for real data and the other for imaginary data; these areas are accessed with the even addresses and odd addresses respectively.

The address ranges shown below test the operand memory IC's, which correspond to the most significant byte and the least significant byte as indicated.

Address Ranges	Most Significant Byte	Least Significant Byte
0-7FF	IC13	IC24
800-FFF	IC14	IC25
1000-17FF	IC60	IC62
1800-1FFF	IC61	IC63

If the address is even, the IC's referred to are on the real ALU (board 9 to the left of board 10).

If the address is odd, the IC's referred to are on the imaginary ALU (board 9 to the right of board 10).

BBBB: expected value. This is always the inverse of the data address.

CCCC: obtained value.

Test 6 DFT

Test 6 is another array processor test and executes an 840 point DFT on a known impluse of data. The result is transferred by direct memory access (DMA) to the RVC memory and checked against the known result data. This verifies the special DFT addressing logic and magnitude latch operation on the multiplier board (board 10).

Error Interpretation:

Test status display:

6 DFT PROC AAAA BBBB CCCC FAILED

AAAA: address of a location of an incorrect value.
This address can range from 0 to 347 (0 to 839 dec.) to include the 840 complex results from the DFT. A value of 348 indicates a failure of the block exponent.

BBBB: expected value;
a value of 800 is a real result
a value of 1000 is an imaginary result
a value of 4001 is the block exponent result.

CCCC: obtained value.

Test 7 TEST STORE

In Test 7, the data stored in the test store is checked for validity. If the data is invalid the test store is cleared and the message 'CLEARED' is included in the status line.

Error interpretation

Test status display:

7 TEST STORE CLEARED

Test 8 GPIB

This test is executed only when the machine is in "local" mode, so as not to disturb the GPIB remote control.

A simple read/write check of the GPIB chip (IC6, board 6) is executed.

Error Interpretation

Test status display:

8 GPIB AAAA BBBB CCCC FAILED

AAAA: address of failed register.

BBBB: expected value.

CCCC: obtained value.

If the 12002A option is not present the message '8 GPIB NOT FITTED' appears.

Test 9 PLOTTER

This is a simple read test of the plotter interface.

Error Interpretation

Test status display:

9 PLOTTER AAAA BBBB CCCC FAILED

AAAA: always 2E28.

BBBB: 0000 (always zero)

CCCC: FFFF (only failure value; any other value is valid).

If the 12003A option is not present the message '9 PLOTTER NOT FITTED' appears.

Test 10 KEYBOARD CODE TEST

This test allows the codes generated by the keyboards to be verified. It is executed only when the machine is in local mode.

The test requires the operator to press each key and to check the generated code characters.

The test is terminated by pressing the ENTER key on the numeric key pad.

Each key generates a sequence of ASCII characters which are equivalent to the remote command codes.

See Fig. 2.4 for the correct codes.

Note that the 'rtl' key has no action in this test and that pressing shift/SELFTEST will terminate the test sequence as normal.

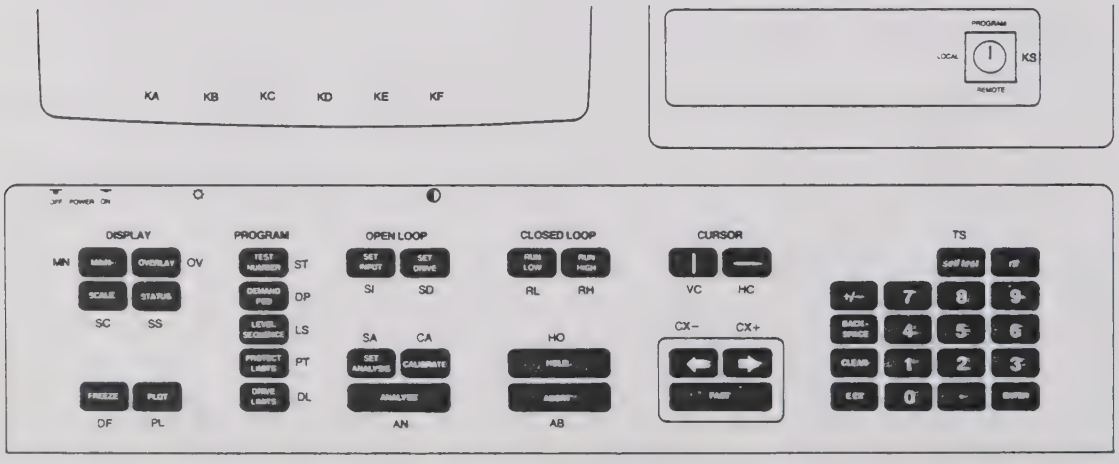

Fig. 2.4 GPIB command codes

Test status display:

10 KEYBOARD PRESS A KEY XXXXX PRESS ENTER TO FINISH

'XXXXX' are the ASCII codes generated by the key pressed.

The number of characters generated varies. Normally two alpha characters plus a terminator (>) are shown. The number keys show only one numberic character, except CLEAR and BS which display ']' and blank respectively. The cursor move keys generate the CX command followed by a number, the value of which varies.

POWER UP TEST : IC NUMBERS

DISPLAY

Address	ICs															
	msb															lsb
8000-BFFE	IC50	36	22	9	51	37	23	10	52	38	24	11	53	39	25	12
	Bd 2															

	Hi byte	Lo byte
C000-C7FE	IC21	IC32
C800-CFFE	IC20	IC31
	Bd 3	Bd 3
D000-D7FE	not used	IC30/Bd 2

SCRATCH RAM

Address	Most Significant Byte	Least Significant Byte
0-7FE	IC59	IC58
800-FFE	IC43	IC42
1000-17FE	IC9	IC7

CHECKSUM
The test writes the failed IC numbers on the display in hexadecimal. All IC numbers refer to Board 28.

DATA RAM

Address	Most Significant Bit	Least Significant Bit
0-3FFF	IC16 IC15 IC14 IC13	IC2 IC1
4000-7FFF	IC32	IC17
8000-BFFF	IC48	IC33

All IC's are on Board 4

ARRAY PROCESSOR

Address	Most Significant Byte	Least Significant Byte
0-7FF	IC13	IC24
800-FFF	IC14	IC25
1000-17FF	IC60	IC62
1800-1FFF	IC61	IC63

If address is even, the IC numbers refer to Real Board 9 (which is to the left of Board 10).
If address is odd, the IC numbers refer to Imaginary Board 9 (which is to the right of Board 10).

CHAPTER 3

RVC SYSTEM BUILD PROCEDURE

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3.1 INTRODUCTION

This system build procedure may be used to diagnose faults to within an area. The procedure provides for the gradual build up of the RVC, from an empty mainframe to a fully functional system, and allows faults to be diagnosed to the same level as that achieved with the self test.

3.2 EQUIPMENT REQUIRED

1. Board 20 diagnostic module.
2. Texas Silent 700 or similar keyboard and terminal.
3. Scope.
4. DVM - Vdc, ohms and Vac (true rms) [eg SOLARTRON 7060E].
5. HP 9825 calculator.
6. Oscillator/function generator (0-100kHz).
7. Board 32 Bus grant continuity module.
8. Clare mains insulation and earth return impedance tester (or similar unit meeting IEC 348).
9. Frequency counter (eg Enertec 2630).
10. Variable ac supply transformer, eg Variac.

WARNING

Extreme care should be used when working on the interior of the RVC while this instrument is, or has recently been, switched ON. Lethal voltages exist in the area of the ac supply circuitry and the CRT display.

TEST PROCEDURE

3.3 BASIC MAINFRAME AND POWER SUPPLIES

Remove all boards, including board 53.

Remove display power and signal cable (PLA)

Check on the ac mains inlet that:

a. A ground is connected.
b. There are no shorts between any pins with mains the power switch ON and OFF.

Check for shorts between ground and:

a. +5V on motherboard
b. +12V on motherboard
c. -12V on motherboard
d. +12V on display connector (PLA)

Connect the RVC to the IEC 348 test set.

Switch ON and check the impedance from the mains earth to the following points using an IEC 348 approved test set operating at 25A. All readings should be < 0.5 ohms.

a. Left and right hand side plates (12000201 and 1200202)

b. Fan finger guard

c. Three tie bars into which case bolts screw (12000217)

d. Fixing screw on blanking panel on rear above slot for GPIB option assembly.

If a satisfactory earth return is found, check insulation leakage at 1.5KV, ensuring current is less than 20mA from live and neutral to earth.

Set the variac to its lowest position. Connect the RVC to the ac mains via the variac, switch ON and slowly increase the voltage up to the setting selected by the rear panel switch.
Check and set (G6-40 PSU) +5 +/-0.1V on motherboard.
Check and set (G12-2.5 PSU) + 12V (Display PLA) +/-0.1V
Check +12V and -12V modules on motherboard.
Check that all cables are correctly routed.
Check that all rear panel connectors are isolated from chassis, except for video output.

3.4 CONTROLLER

Insert Board 1 and a tested and proved Board 20. Ensure that watch-dog is OFF (SW2) and diagnostics ON (toggle 1 SW1 ON, other toggles OFF).

Connect the Silent 700 to board 20.

Switch on the RVC. Pressing BOOT SWITCH on board 20 should cause normal S-BUG prompt to be printed:-

```
WP:0000  PC:0000   ST:0000
S >
```

Use S-BUG to access scratch pad RAM as a quick operational check.

```
ie. S > 0/
0000: xxxx          1234 <space>
0000: 1234            etc
```

Access adresses #0, #800 and #1000 to test the three banks of RAM.

Switch the RVC OFF.

3.5 DISPLAY

Plug in Boards 2 and 3

Plug in Display Power and Signal cable.

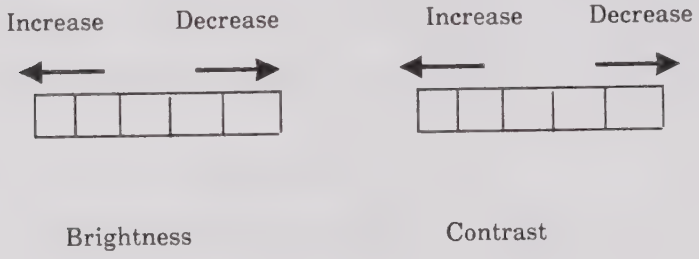
Ensure frame rate selected on Board 2 is in accordance with local mains supply. (SWA)

Switch the RVC ON.

Press the BOOT switch on Board 20 to initialise the display.

Adjust the brightness and contrast controls, on the front panel, the horizontal frequency control (VP1009) and the vertical hold control (VP1300) to view the Solartron logo.

Check the orientation of the brightness and contrast controls.



3.5.1 Display Boot

Insert bus grant continuity plug (Board32) into Board 51 SKB.

Using S-BUG access the display control register and manually boot the display ie,

```
S > FF40/M

FF40: X X X X      100 <space>
FF40: 0 0 C 0
```

This will cause the logo to flash and tests both the display boards and access to the 1200 bus. Check that the 1200 bus time out LED does not light during this access.

3.5.2 CRT Adjustment

Using S-BUG, command the display to give a cross hatch pattern ie. Press Boot Switch on Board 20

```
S > EC00 / M

EC00: XXXX        5 <LF>
EC01: XXXX       36 <LF>
EC02: XXXX       11 <LF>
EC03: XXXX     F000 <LF>
EC04: XXXX       4C <RET>

S > FF40/M

FF40: OOCO     1 <space>
FF40: XXXX     -
```

Using the following adjustments ensure that the cross hatch appears centrally in the whole display area with good linearity and focus.

The digivision CRT modules are factory pre-aligned and should need only minor adjustment to produce an acceptable display. The entire alignment procedure should only take 10-15 minutes. Acceptable picture geometry can be readily assessed using the cross-hatch pattern, such that all lines are straight to within +/-2mm over the screen width and height and all boxes are of identical size to within +/-1mm.

The picture size and position are best adjusted using the normal display produced by executing the system program (x7000) and pressing the demand psd menu key. The gap between the display and edge of the moulding measured at the mid-point should be 5mm +/-2mm on all four sides and the soft key boxes shouuld align with the keys to within +/-2mm.

Note: Suitable safety precautions are necessary to avoid high voltage shock and tube implosion.

WARNING:DUE TO LETHAL VOLTAGES PRESENT EXTREME CAUTION IS NEEDED WHEN PERFORMING CRT ADJUSTMENTS

Phase control (VP1008),
Adjust this to mid-point initially and then use as a fine horizontal position control.

Picture Width (VP1008)
This may be adjusted by turning the ferrite screw core in L1 using a suitable plastic trimming tool.

Picture Height(PVP1300)
A preset potentiometer P4 with thumbwheel may be turned to adjust height.

Picture Geometry (squareness)
Small round magnets are provided which locate on spigots surrounding the scanning yoke and these can be added and rotated for best raster shape.

Picture Position (or centering)
Two radial magnets fitted on the scanning yoke can be rotated individually or together as required to center the raster on the screen.

Vertical Linearity(VP1300)
A preset control P5 can be adjusted using a fine screwdriver to balance linearity at the top of the picture to that at the bottom of the picture .

Horizontal Linearity
It is necessary to set up each monitor so that the cross hatch squares on the left and right hand sides of the screen are the same width and to do this the linearity sleeve fitted in the scan yoke assembly must be pushed in or pulled out. The more the sleeve is pushed in the more the squares on the left are crushed. Balance between left and right should be obtained.

The linearity sleeve is a tight fit between the CRT neck and the scanning yoke. Firm steady pressure must be applied when fitting or adjusting the linearity sleeve. Always fit the linearity sleeve inside the scanning yoke prior to assembling onto the CRT neck.

Vertical Hold(VP1300)
Adjust P3 to the mid position between loss of lock points .

Horizontal Frequency(VP1008)
Adjust to mid lock position.

3.5.3 Video Output

Check the video output on the rear panel BNC connector using a scope.
Switch off the RVC.

3.6 CONTROL PROGRAM

If board 28 is not fitted, then omit this section and continue at 3.7.

Check Board 28, visually, for solder bridges, incorrectly fitted IC's etc.

Add correctly programmed PROM's

Plug Board 28 into rack.

Ensure bus grant module is fitted to Board 51, SKB

Switch the RVC ON. Using S-BUG execute the system program to invokethe power up test. ie

S > X7000 <ret>

If board 28 is functioning correctly the CRT will display:-

POWER UP TEST

	POWER UP TEST	SYSTEM S/W ISSUE
1. DISPLAY	PASSED	DISPLAY S/W ISSUE
2. SCRATCH RAM	PASSED	
3. CHECK SUM	PASSED	
4. DATA RAM 0000 0000 FFFF	FAILED PRESS	

Switch the RVC off.

3.7 DATA RAM

If Board 28 is not fitted into the unit, then insert programmed ICs into Board 4.and plug in Board 4.

Ensure bus grant module is fitted to Board51 SKB

Switch the RVC ON

Execute the system power up test as described above (Use S-Bug X7000 command). The CRT will display:-

	POWER UP TEST	SYSTEM S/W ISSUE	
1.	DISPLAY	PASSED	DISPLAY S/W ISSUE
2.	SCRATCH RAM	PASSED	
3.	CHECK SUM	PASSED	
4.	DATA RAM	PASSED	
5.	ARRAY PROC.		

Switch the RVC OFF.

3.8 ARRAY PROCESSOR

Plug in Boards 8, 9 (2 off) and 10

Ensure bus grant module is fitted to Board51 SKB

Switch the RVC ON.

Execute the system power up test as described above (Use S-BUG X7000command). The CRT will display:-

	POWER UP TEST	SYSTEM S/W ISSUE	
1.	DISPLAY	PASSED	DISPLAY S/W ISSUE
2.	SCRATCH RAM	PASSED	
3.	CHECKSUM	PASSED	
4.	DATA RAM	PASSED	
5.	ARRAY PROC.	PASSED	ARRAY P.S/W ISSUE
6.	DFT PROC	PASSED	
7.	TEST STORE	TEST STORE CLEARED	

Items 5 and 6 relate to the boards 8, 9 and 10
On failure refer to test program diagnostic information and individual board test procedures.

Switch the RVC OFF.

3.9 INPUT AND GENERATOR SYSTEMS

Plug in Boards 51 and 52. Ensure split pads (SP1 to SP10) on Board 51 are made.

Switch the RVC ON.

Execute the system power up test as described above. (Use S-BUG X7000command)

All of the power up tests should pass. The default machine operation will start automatically after a successful power up test. On failure refer to the power up test diagnostic information and the individual board test procedures.

Check that the "BUSY" LED's on boards 3 and 8 flash ON/OFF in the normal sequence when the system software is running.

3.10 FRONT PANEL

Check the position and orientation of all flexible cables connecting to Board 53 socket (especially the power cable). Plug board 53 in on an extension card. Connect the cables to SKI (4 way)and SK2 (26 way) connectors on Board 3.

Check the Baud rate osciallator frequency using a frequency counter connected to TP10. Adjust RV1 to give a frequency of 77kHz +/-2kHz.

Execute the system program (using S-BUG X7000 command). Check that a long bleep is heard immediately the power up test starts.

Check that both duralith panels cause a short bleep and that LED 1 is only alight when a key is pressed.

Set the keyswitch to PROGRAM and check that each key on the main keyboard selects the correct function.

Set the keyswitch to local and check that the status information at the top left of the display (2nd line down) reads "LOC".

Set the keyswitch to REMOTE and check status changes to "REM"

Return the keyswitch to PROGRAM and check status returns to "PRGM"

Select the SCALE menu. Check that each soft key operates correctly. Using the DATA AXIS key, check that both shift keys operate, ie that the sequence g ^{2}/Hz, g/$\sqrt{}$Hz, LOG, SI PSD, SI ASD, SI LOG progresses forward with no shift and in reverse with shift.

Check the operation of the cursor "FAST" key.

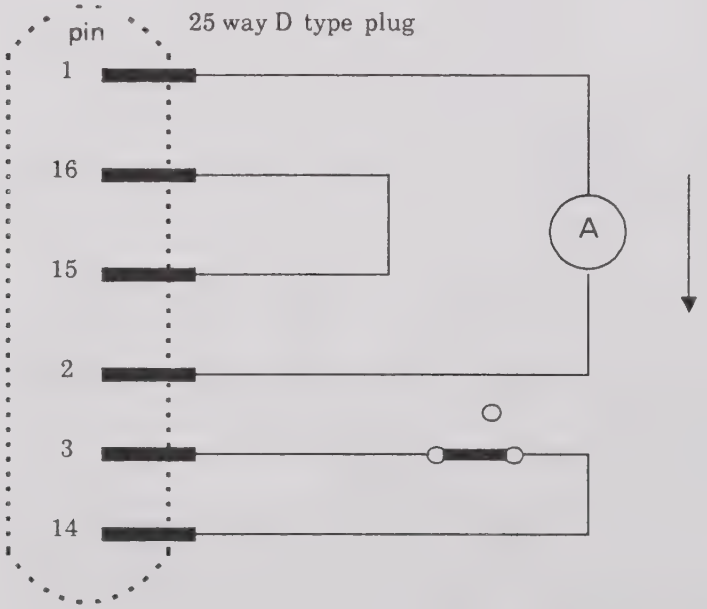


Fig 3.1. Dummy interlock plug

Fit a dummy interlock plug (wired as in figure 3.1) in the interlock socket on the rear panel. With the ammeter connected acrosss pins 1 and 2 and pins 3 and 14 s/c (SW on) check that the ammeter reads 20mA +/-4m/a. Also check system status gives "interlock status request/ready". O/C pins 3 and 14 (SW OFF) check that the ammeter reads OmA +/-1mA. Check that the error message "Terminated Externally" is given and that system status reads "interlock status abort/ready".

3.11 ANALOG INPUT/OUTPUT CABLES

Ensure that each of the four cables is correctly positioned on Board 52.

Run the system program

Press Calibrate key
Select DRIVE
Set FREQUENCY = 480Hz AND PEAK G = 5
Select LEVEL
Set VPEAK = 5

Select "DISPLAY MAIN" "TEST SIGNAL"

Check individually the following signal paths

a. 'Scope monitor to voltage input Hi
b. 'Scope monitor to voltage input Lo
c. 'Scope monitor to charge input (via 1000pF capacitor)
d. 'Generator Hi/Lo to voltage input Hi/Lo

Display should show a sigle sinewave.

Press "INITIALISE" followed by "CLEAR ALL TESTS" (in the self-test menu).

3.12 SCANNER MODULE TEST

If the scanner option (12101A) is not to be fitted, continue with the next section of this spec.

Set SW1 on the scanner card to position "0" (slot horizontal and arrow pointing upwards).
Set RV1 on the scanner card fully anticlockwise.

Switch RVC OFF.

Insert scanner module into RVC frame in uppermost option slot and connect cable (either way round) between the scanner card and the socket on board 51, routeing carefully.

Switch RVC on

Press "SET ANALYSIS" and check that six soft keys are displayed. If the scanner is faulty, or incorrectly fitted, only the leftmost four keys will appear.

3.13 FINAL TEST

This assumes all the above checks have been completed

Remove Board 20 - diagnostic module

Ensure all toggles are OFF on SW1 board 1

Ensure watch-dog in ON, SW2 board 1

Switch mains power ON

Check that all power up tests pass - indicated by automatic entry to the normal machine operation.

CHAPTER 4

RVC CALIBRATION PROCEDURE

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CHAPTER 4 RVC CALIBRATION PROCEDURE

4.1 INTRODUCTION

The calibration procedure described in this chapter assumes that the RVC is fully operational.

Prior to calibration the RVC should be switched on for at least 15 minutes to allow the instrument to warm up. Also, the calibration should be performed with all boards inserted, except where stated otherwise.

Section 4.3, 'Frequency Calibration', may be performed independently, but Sections 4.4 to 4.9 should be performed in succession in the order given.

To ensure full serviceability of the RVC the calibration procedure should be followed by the RVC check procedure described in Chapter 5.

4.2 EQUIPMENT REQUIRED

1. RVC complete working system.
2. DVM, 1μV to 10V ac/dc true rms, e.g. Solartron 7060E.
3. Frequency counter, resolution and accuracy < .0003%).
4. Extension board.
5. Sine wave generator, 1kHz.

4.3 FREQUENCY CALIBRATION (Board 51)

4.3.1 With the ac supply switched off, insert board 51 into the RVC mainframe on the extension board.

4.3.2 Switch on the ac supply.

4.3.3 Connect the frequency counter between test point TP1 and ground.

4.3.4 Adjust CV1 so that frequency = 16,128,000 Hz ± 200Hz.

4.3.5 Switch the power off and on and check that the oscillator starts reliably.

4.3.6 Disconnect the frequency counter from test point TP1.

4.3.7 Switch off the ac supply.

4.3.8 Remove board 51 and the extension board and then insert board 51 directly into the mainframe.

4.4 DC OFFSET ADJUSTMENT (Board 52)

4.4.1 With the ac supply switched off, disconnect the cables connecting board 52 to the rear panel connectors. Remove the board from the RVC mainframe, and re-insert into the mainframe on the extension board. All screens must be fitted. Reconnect board 52 to the rear panel connectors, using the following extension leads:

voltage input cable
charge input cable
monitor output cable
generator output cable

4.4.2 Switch on the ac supply.

4.4.3 Allow board 52 to 'warm up' for at least 15 minutes before proceeding any further with the calibration procedure.

4.4.4 Select the SYSTEM CHECK via the SELF TEST menu. The RVC should pass all tests.

4.4.5 Select the INIT STORE menu and press the CLEAR ALL TESTS soft key. ("INIT STORE" IS TO DEPRESS MENU/SELFTEST SOFT KEY IN SELF TEST MENU)

4.4.6 Select the SET INPUT menu and set:

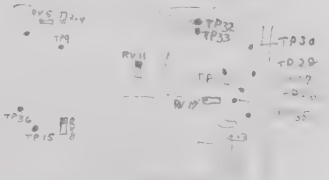
a) RANGING	Fixed,
b) RANGE	10mV.

4.4.7 Link the voltage Hi and Lo inputs together. CHECK LINK ON BACK — RS232 CONNECTOR INTERLOCK

4.4.8 Select ANALYSE.

4.4.9 Monitor each of the following test points in turn with the DVM and adjust the associated preset control for minimum reading on dc volts. TP-1 = GROUND ≈ LESS THAN 1 MV

Test Point	Control
TP9	RV4
TP36	RV5
TP15	RV8 — FOR MINIMUM EG 90 mV



4.4.10 Select the SET INPUT menu and set:

a) ACCL TYPE	pC/g,
b) Lo INPUT	Grounded.

4.4.11 Link the charge input to ground, via a 1000pF capacitor (tolerance 1% or better; Solartron part no. 208500057).

4.4.12 Monitor test point TP36 with the DVM and adjust preset control RV11 for minimum reading.

4.4.12 Insert a link bween test point TP35 and zero volts. TP-1

4.4.13 Select SYSTEM INITIALISE (via the SELF TEST menu), then ANALYSE.

4.4.14 Monitor each of the following test points in turn with the DVM and adjust the associated preset control for minimum reading.

Test Point	Control
TP26	RV17
TP27	RV18
TP28	RV20
TP30	RV21

4.4.15 Remove the link previously connected between test point TP35 and zero volts.

4.4.16 Set toggle 5 of switch S1 on board 1 to 'ON'.

4.4.17 Select SYSTEM INITIALISE, then ANALYSE.

4.4.18 Monitor test point TP30 with the DVM and adjust preset resistor RV19 for minimum reading.

4.4.19 Set toggle 5 of switch S1 on board 1 to 'OFF'.

4.4.20 Select SYSTEM INITIALISE, then ANALYSE.

4.4.21 Connect a link between test point TP33 and zero volts.

4.4.22 Monitor test point TP32 with the DVM and adjust preset control RV24 for minimum reading.

4.4.23 Remove the link previously connected between test point TP33 and zero volts.

4.4.24 Connect a link between test point TP32 and zero volts.

4.4.25 Monitor test point TP33 with the DVM and adjust preset control RV23 for minimum reading.

4.4.26 Remove the link previously connected between test point TP32 and zero volts.

4.4.27 Monitor test point TP34 with a DVM and adjust preset control RV25 for minimum reading.

4.4.28 Repeat steps 4.4.21 to 4.4.27 inclusive until all readings are as close to 0V dc as possible and not greater than ±1mV.

4.5 GENERATOR AMPLITUDE CALIBRATION (Board 52)

4.5.1 Connect the DVM (set to true rms ac volts) to the generator monitor output. Use extender cable to link output cable to SK4.

4.5.2 Select SYSTEM INITIALISE, then CALIBRATE.

4.5.3 Select the CALIBRATE DRIVE menu and set:

a) FREQ (Hz)	102,
b) g PEAK	7.071.

4.5.4 Select the CALIBRATE LEVEL menu and set:

V PEAK	7.071.

4.5.5 Adjust preset control RV16 until the DVM reads 5.00 ± 0.001 Vrms.

4.5.6 Select the CALIBRATE DRIVE menu and set:

FREQ (Hz)	2988.

4.5.7 Select the CALIBRATE LEVEL menu and set:

V PEAK	8.25.

4.5.8 Check that the DVM reads 5.00 ± 0.05 Vrms.

4.6 LOW FREQUENCY AMPLITUDE CALIBRATION OF THE VOLTAGE INPUT (Board 52)

4.6.1 Switch off the ac power supply.

4.6.2 Remove the extension cables from board 52. Ensure that board 52 screens are fitted. Remove board 52 and the extension board from the RVC mainframe and then insert board 52 directly into the mainframe. Remove the extension cables from the rear panel cables and reconnect the rear panel cables directly to sockets SK1 - SK4 on board 52.

4.6.3 Connect the generator Hi output to the voltage Hi input and the generator Lo output to the voltage Lo input.

4.6.4 Select the SET INPUT menu and set:

a) ACCL TYPE	mV/g,
b) RANGING	Auto,
c) Lo INPUT	Active.

4.6.5 Select the CALIBRATE DRIVE menu and set:

a) FREQ (Hz)	102.
b) g PEAK	7.071

4.6.6 Select the CALIBRATE LEVEL menu and set:

V PEAK	7.071.

4.6.7 Select the SET INPUT menu.

4.6.8 Adjust preset control RV3 such that the accelerometer sensitivity value displayed is 1000±1.

4.6.9 Connect the generator Lo output to zero volts and the generator Hi output to the voltage Hi and Lo inputs.

4.6.10 Select the SET INPUT menu and set:

a) RANGING	Fixed,
b) RANGE	10mV.

4.6.11 Adjust preset control RV1 for a minimum accelerometer sensitivity value, which should be <1.

4.7 HIGH FREQUENCY AMPLITUDE CALIBRATION OF THE VOLTAGE INPUT(Board 52)

4.7.1 Using the SET INPUT menu, select AUTO RANGING.

4.7.2 Link the generator Hi output to the voltage Hi input and the generator Lo output to the voltage Lo input.

4.7.3 Select the CALIBRATE DRIVE menu and set:

FREQ (Hz)	2988.

4.7.4 Select the CALIBRATE LEVEL menu and vary the Vpk value to obtain a DVM reading of 5.00 ± 0.01 volts. (DVM is connected to generator monitor output.)

4.7.5 Using the SET INPUT menu, adjust preset control C2 to obtain an accelerometer sensitivity value of 1000 ± 5. Note that the addition or removal of C98 and/or C99 may be required to achieve this value.

4.7.6 Link the generator Hi output to the voltage Hi and Lo inputs, and the generator Lo output to zero volts.

4.7.7 Using the SET INPUT menu, select the fixed 10mV range.

4.7.8 Adjust preset control C3 for a minimum accelerometer sensitivity value, which should be <1.

4.8 CHARGE AMPLIFIER CALIBRATION (Board 52)

4.8.1 Using the SELF TEST menu, select SYSTEM INITIALISE.

4.8.2 Using the SET INPUT menu, select pC/g and AUTO RANGING.

4.8.3 Select the CALIBRATE DRIVE menu and set:

a) FREQ (Hz)	1500.
b) g PEAK	7.071

4.8.4 Select the CALIBRATE LEVEL menu and vary the Vpk value to obtain a DVM reading of 5V ± .01 volts. (DVM is connected to generator monitor output.)

4.8.5 Link the generator monitor output, via a 1000pF capacitor (tolerance 1% or better; part no. 208500057), to the charge input.

4.8.6 Select the SET INPUT menu and adjust preset control RV2 to obtain an accelerometer sensitivity value of 1000 ± 5.

4.8.7 Remove the links connected in steps ~~4.8.2~~ 4.7.6 and ~~4.8.3~~ 4.8.5.

4.9 OVERLOADS (Board 52)

4.9.1 Using the SELF TEST menu, select SYSTEM INITIALISE, followed by CLEAR ALL TESTS.

4.9.2 Set preset controls RV6 and RV7 fully anticlockwise.

4.9.3 Connect the voltage Hi and Lo inputs, in parallel, to the output of the sinewave generator. Set the frequency of the generator output to 1kHz and the amplitude to 11Vpk (7.8V rms).

USE SG5010A

4.9.4 Using the SET INPUT menu, select mV/g and the FIXED 10mV range.

4.9.5 Select ANALYSE.

4.9.6 Carefully adjust preset control RV6 to the precise point at which the error message 'CM/HF OVERLOAD' disappears from the display.

& INPUT OVERLOAD COMES ON.

4.9.7 Set the frequency of the generator output to 10kHz and the amplitude to 15mV rms.

4.9.8 Using the SET INPUT menu, select 'Lo INPUT GROUNDED'.

4.9.9 Carefully adjust preset control RV7 to the precise point at which the error message 'CM/HF OVERLOAD' appears on the display.

CHAPTER 5

RVC CHECK PROCEDURE

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5.1 INTRODUCTION

This check procedure should follow the System Build and Calibration procedures. This procedure is performed with the RVC in its case and provides a full check of all RVC functions. A form for recording the test results is given at the end of this chapter.

5.2 EQUIPMENT REQUIRED

Attenuator 0-1/(1024) in 1/(2) Steps or decade divider x1 to x0.001.

Oscilloscope

Function generator 0-100kHz sine/square

8 digit counter (.0005% accuracy)

True rms DVM (eg Solartron 7060E)

Bryans 8700 plotter and 12002A GPIB Interface

Test Program 12105300

Video monitor or video or video platter

Scanner test box 12106800 (Only if Scanner Module is fitted)

5.3 PRE-TEST PROCEDURE

Ensure that the RVC has been calibrated and passed a System Build Test

Ensuer that the RVC is NOT connected to an ac mains supply.

Check that all internal mechanical items, boards, cables, clamps and connectors are correctly in place.

Check that SW1 on Board 3 is in the 50Hz position

Check on Board 1 that all toggles on SW1 are set to OFF and that SW2 (Watchdog) is set to ON

Check for correct complement of boards All diagnostic boards, such as Board 20, should be removed.

Fit the RVC case to the mainframe.

5.4 POWER ON

With the power switch on the RVC front panel set to OFF, connect the instrument to an ac supply.

Switch the RVC to ON and check that machine powers up correctly, first time, and that the power up test runs. with no errors and enters the stand-by operating state.

Check that no errors occur during the power up test and that the normal default machine operation is entered.

5.5 DISPLAY

Check display alignment and linearity. The display view should be central in CRT and there should be very little pin cushion distortion or astigmatism.

Select Set INPUT menu. The menu keys should line up correctly with the menu on the CRT and there should be no loss of picture at either side of the menu.

Select the vertical cursor and check the following:

a. The cursor movement keys ← and → cause, when pressed, the cursor to move to the left and right respectively.
b. Pressing the FAST key in conjunction with either cursor movement key causes the cursor to move faster, and still gives smooth control.

Select the horizontal cursor and check the following:

a. The cursor movement keys ← and → cause, when pressed, the cursor to move up and down respectively.
b. Pressing the FAST key in conjunction with either cursor movement key causes the cursor to move faster, and still gives smooth control.
c. No cursor break-up occurs and the cursor appears at all positions on the display.
d. The cursor length and orientation conform with the graph outline.

5.6 SELF TEST AND KEYBOARD

Execute the user SELF TEST function in the Self Test menu.

Ensure that the RVC passes all tests successfully, up to the final test.

When the final keyboard test is entered test each key displays its correct ASCII code on the display. Check the menu and shift keys also .

5.7 INPUT NOISE FLOOR

Initialise the RVC and clear all tests using the SELF TEST menu.

Short circuit the voltage input Hi and Lo to ground.

Short circuit Charge input via a 1000pF capacitor.

Select mV/g on the Set Input menu.

Select AVERAGE PSD display function using the DISPLAY MAIN menu key.

Select FIXED Input range.

Ensure that the residual noise level is below the values given for each range in Table 5.1.

Select SCALE, DATA AXIS, LOG

Press SET ANALYSIS key and enter Test Decay = 10

Press Analyse.

Select the ranges indicated below and press AVERAGE RESET after each change of range.

Table 5.1

RANGE	NOISE LIMIT	
	mV/g	pC/g
10mV	-100	-110
20mV	-100	-110
40mV	-100	-110
80mV	-100	-110
0.16V	-100	-105
0.31V	-95	-100
0.62V	-90	-100
1.25V	-90	-95
2.50V	-85	-90
5.00V	-85	-85
10.00V	-80	-80

Record results

Repeat for pC/g Input

NOTE: Measurements should be taken on highest peak on the display.

Remove the 0V short from the Hi and Lo inputs. Remove the shorting capacitor from the Charge input.

5.8 CALIBRATION

Initialise the RVC using the SELF TEST menu , then select CLEAR ALL TESTS

Connect a DVM to the Scope Monitor output.

Connect generator Hi and Lo to Voltage input Hi and Lo respectively.

Select Set Input menu and select as follows:-

Accl type - mV/g
Accl sens - 1000
Ranging - Auto
Lo I nput - Active

* Press CALIBRATE Key

Select LEVEL and enter VPEAK = 7.071

Select DRIVE and enter FREQUENCY = 102

Select gPEAK = 7.071

Check and record the generator output voltage on the DVM this should be 5.00 +/- 0.01volts. Check and record the ACCL SENS displayed in the set input menu. This should be 1000+/- 20.

Press Calibrate Key and select DRIVE

Enter FREQUENCY = 2988

Check and record the generator output voltage on the DVM this should be 4.308 +/- 0.06volts. Check and record the "ACCL SENS" displayed in the set input menu. This should be 862 +/- 25.

Connect monitor to charge input via 1000pF 1% capacitor (leave the DVM connected).

Select Set Input menu and set up as follows:-

Accl type - pC/g
Accl sens - 1000
Ranging - Auto
Lo Input - Grounded

Repeat from *.

5.9 RANGE TO RANGE INPUT CALIBRATION

Press INITIALISE followed by CLEAR ALL TESTS.

Connect the Monitor output to the attenuator or divider box.

Connect the HI input to the attenuator or divider box output.

Connect a true rms reading as DVM to the monitor output. (Suitable DVM is Solartron7060E)

Press CALIBRATE key

Select LEVEL and enter VPEAK = 5.12 if a binary attenuator is used or 5.00 if a decade divider is used.

Select DRIVE and enter FREQUENCY = 102

Select gPEAK = 0.005

Select "Set Input" menu and set up as follows:-

Accl type - mV/g
Ranging - Fixed
Range - 10mV
Lo Input - Grounded

For the set up range, attenuator and gPEAK settings check and record the displayed ACCL SENS in the set input menu. This should be 1000 +/- 20 in all cases. 980 - 1020

Check and record the DVM reading. This should be 3.62 +/- 0.02V (binary attenuator) or3.54 +/- 0.02V (decade divider) in each case. 3.52 - 3.56

Table 5.2

RANGE	ATTENUATOR SETTING	gPEAK	DECADE DIVIDER SETTING	gPEAK
10mV	1/(1024)	0.005	x0.001	0.005
20mV	1/(512)	0.01	x0.002	0.01
40mV	1/(256)	0.02	x0.005	0.025
80mV	1/(128)	0.04	x0.01	0.05
160mV	1/(64)	0.08	x0.02	0.01
0.31V	1/(32)	0.16	x0.04	0.2
0.62V	1/(16)	0.32	x0.08	0.4
1.20V	1/(8)	0.64	x0.1	0.5
2.50V	1/(4	1.28	x0.2	1.0
5.00V	1/(2)	2.56	x0.5	2.5
10.00V	1/(1)	5.12	x1.0	5.0

5.10 COMMON MODE REJECTION

Initialise the RVC and clear all tests.

Connect the Generator HI output to both the Voltage Hi and Lo Inputs, taking care that the signal paths to the two voltage inputs are of similar length and routeing. Short the Generator LO output to ground.

Select Set Input menu and set up as follows:-

Accl type - mV/g
Ranging - Fixed
Range - 10mV
Lo Input - Active

Press CALIBRATE Key

Select LEVEL and enter VPEAK = 5

Select DRIVE and enter FREQUENCY = 102 and gPEAK = 5

Check and record the displayed ACCL SENS in Set Imput menu.

Press CALIBRATE key

Select DRIVE and enter FREQUENCY = 2988

Check and record the displayed ACCL SENS in Set Input menu.

In both cases above the displayed ACCL SENS should be less than 1.0.

5.11 OVERLOADS CHECK

Initialise the RVC and clear all tests.

Common mode overload

Connect both the Voltage Hi and Lo Inputs to the HI output of a sinewave oscillator.

Connect the LO output of the oscillator to the ground of the RVC. Set the Osciallator to 1kHz.

Select Set Input menu and set up as follows:-

Accl type - mV/g
Accl sens - 1000
Ranging - Fixed
Range - 10mV
Lo Input - Active

Press ANALYSE

Gradually increase the amplitude of the sinewave until "Error : Common Mode/HF Overload" is displayed. Check and record the amplitude of the sinewave. It should be 11V +/-2V. (PEAK) or 6.4V - 9.2V (rms). Change range to 10mV fixed.

HF Overload

Select 10mV fixed range.

Set the Lo Input Key in the Set Input Menu to Grounded

Set the frequency of the oscillator to 10kHz. Gradually increase the amplitude of the sinewave from zero until "Error : Common Mode/HF Overload" is displayed. Check and record the amplitude of the sinewave. It should be 15mV +/- 5mV rms.

5.12 FREQUENCY ACCURACY

Using the SELF TEST menu, initialise RVC

Connect a frequency counter to the monitor output

Press CALIBRATE key

Select LEVEL and enter VPEAK = 5

Select DRIVE and enter FREQUENCY = 3000 and gPEAK = 5

Check and record the measured Period on the counter. This should be 333.33us +/- 0.01us.

5.13 NON-VOLATILE CONTROL STORE

Enter one set of controller settings into the non-volatile memory store eg DEMANDPSD Freq (Hz) 6, PSD g 2/Hz = 1, Freq (Hz) 3000 & PSD g 2/Hz = 10, a ramp should be displayed. Switch mains supply off and on again twice. Check that the display shows the same ramp.

5.14 PLOTTER

Connect an 8700 plotter or equivalent to the plotter interface.

Switch RVC on.

Using the SELF TEST menu, initialise the RVC

Connect the generator Hi output to the voltage Hi input and connect the generator Lo output to the voltage Lo input

Press MAIN key

Select TEST SIGNAL for display

Press CALIBRATE key

Select LEVEL and enter vPEAK = 5

Select DRIVE and Enter FREQUENCY = 300Hz and G PEAK = 5

Using the plot menu select PLOTTER ANALOG, followed by PLOT ZERO and PLOT FULL SCALE to calibrate the plotter.

Plot the display in A4 mode with annotation.

Check plots for linearity and correct pen up/down control

5.15 GPIB

Switch RVC off and ensure that all GPIB rear panel switches are in the OFF position. This selects address 0, talk only OFF and parallel poll bit 0.

Inset 12002A GPIB interface into RVC and switch RVC on

Select STATUS GPIB

Check GPIB status page for the following:-

Option 12002A	Fitted
Control	Local
Address status	Idle
ASCII address	0
BINARY address	1
SERIAL POLL byte	00000000
PARALLEL POLL	bit 0 False

Connect HP9825/a calculator and execute RVC test program (Part number 12105300)

5.16 SCANNER MODULE

Switch RVC off

Ensure scanner card is correctly fitted and has SW1 set to position "0" (slot horizontal and arrow upwards) and RV1 fully anticlockwise.

Connect test box (12106800) as follows:

Generator monitor out to test box "IN"
Test box cables 1 to 8 to scanner inputs 1 to 8
Scanner "OUT" to input voltage "HI" and 'scope

Switch RVC on

Initialise RVC and clear all tests then select the following settings:

SET INPUT, lo input GROUNDED
SET ANALYSIS, end scan = 8

CALIBRATE, set drive, frequency = 1200, g peak = 1
CALIBRATE, set level, V peak = 1
DISPLAY MAIN, test signal

The display should show a sine wave whose amplitude has the envelope of a decreasing ramp.

Check on the scope that the total time for a period of the ramp is 12ms +/-6ms

Set RV1 fully clockwise

Check on the scope that the total time for a period of the ramp is 2s +/-1s. Eight distinct levels should be seen in the ramp.

Set SW1 on scanner to position 2 (2 clicks clockwise).

Set up the following:-

ABORT
SELF TEST, INITIALISE
SELF TEST, CLEAR ALL TESTS
ANALYSE
SET DRIVE, FLAT PROFILE, drive grms = 1
DRIVE LIMITS, safe V peak = 10
SET ANALYSIS, end scan = 8, test decay = 30

Allow 1 minute for the value to settle and then check that the displayed AVG g figure at the top of the screen is 0.6g +/-0.06g.

Serial No.....

5.7 INPUT NOISE FLOOR

Range	mV/g	pC/g	Noise mV/g	Noise pC/g
10mV			-100	-110 dB
20mV			-100	-110
40mV			-100	-110
80mV			-100	-110
0.16Vm			-100	-105
0.31V			-95	-100
0.62V			-90	-100
1.2V			-90	-95
2.5V			-85	-90
5V			-85	-85
10V			-80	-80

5.8 CALIBRATION

		mV/g	pC/g
Generator Output	102Hz		5.00V +/- 0.01V
	2988Hz		4.308V +/- 0.06V

		mV/g	pC/g
Sensitivity	102Hz		1000 +/- 20
	2988Hz		862 +/- 25

5.9 RANGE TO RANGE INPUT CALIBRATION

Range	Sensitivity	DVM
10mV		
20mV		
40mV		
80mV		
0.16V		1000 +/- 20
0.31V		
0.62V		
1.2V		
2.5V		
5V		
10V		

5.10 COMMON MODE

	Sensitivity
102 Hz	1.0
2988Hz	

Overloads Check

Common Mode	6.4 to 9.2Vrms
HF	15mV +/-5mVrms

5.12 FREQUENCY ACCURACY

3kHz sine	333.33us +/- 0.01us

CHAPTER 6

SYSTEM DESCRIPTION

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6. SYSTEM DESCRIPTION

6.1 INTRODUCTION

The RVC System consists of the operational modules shown in Fig. 6.1. Data flows through the system under the supervision of the CONTROLLER, which operates in accordance with the local or remote commands. Local commands are applied to the controller via the front panel keys and the KEYBOARD INTERFACE, whilst remote commands are applied via the GPIB INTERFACE.

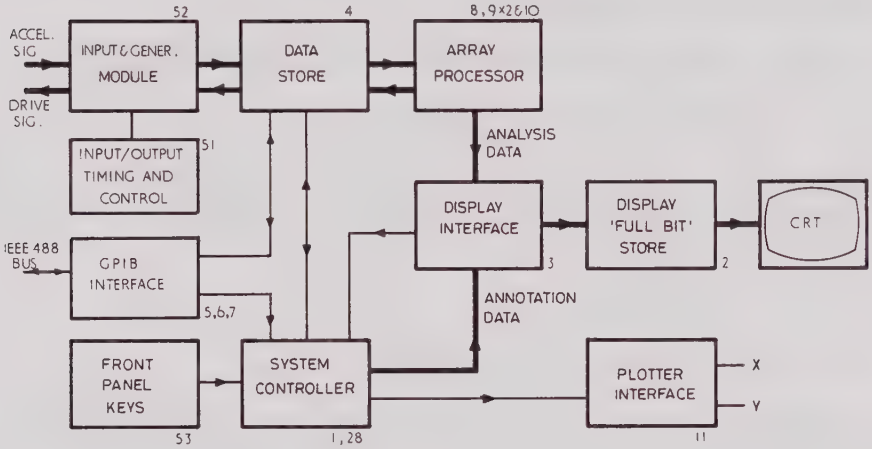

Fig 6.1 System dataflow.

6.2 DATA FLOW

The data flow involves the transference of data from module to module by direct memory access (DMA). These transfers take place on the RVC bus and four modules are capable of controlling them - the input and generator module, the system controller, the array processor and the GPIB interface. The main function of the system controller is to set up the operational parameters of each of the other DMA controlling modules, in accordance with the control commands. The use of the RVC bus is shared by the DMA controlling modules in accordance with a fixed priority structure and bus 'mastery' passes from one to the other as operation progresses. (Further information on the RVC bus is given in Chapter 7).

A filtered random signal is output by the GENERATOR section of the Input and Generator module and is applied to the system under test, via a power amplifier and an electromechanical shaker. The resultant vibration is monitored via an accelerometer and the output of this is applied to the INPUT section. Here, the signal undergoes several stages of processing to obtain time data suitable for analysis. First (on board 52) the input signal is subject to:

* amplification, in accordance with the input range selected.

* anti-alias filtering: attenuation at frequencies greater than 3kHz.

* sampling, to obtain discrete time data

* analogue to digital conversion.

The digital time data thus obtained are transferred to a circular buffer in the DATA STORE under the DMA control of the input module.

6.3 DATA PROCESSING

Time data are transformed into spectral data, and analysis functions computed, by the ARRAY PROCESSOR. This module executes arithmetic operations on arrays of data and, as bus master, is constantly transferring data between the data store and itself in performing the following functions:

* transformation of time data into complex spectral data (instantaneous results stored in data store)

* averaging (average result stored in array processor, on board 9).

* computation of analysis functions (stored in data store).

* computation of co-ordinates for analysis display (results transferred under DMA control of array processor to DISPLAY INTERFACE, memory location E800).

* control of the adaptive loop

* generation of random drive waveform

The test signal is converted to psd (power spectral density) and compared with the demand profile. In closed loop (run) mode, this comparison is used to modify the drive psd according to:

$$\text{drive}(\text{time}_{n+1}) = \alpha(\text{drive}(\text{time}_n)) + (1 - \alpha)\left(\frac{\text{drive}(\text{time}_n) \times \text{demand}}{\text{test}(\text{time}_n)}\right)$$

where α is the averaging constant used to control the rate of loop adaption.

The test psd is also averaged to provide smoothed displays of psd, loop error and transfer function.

The drive psd is randomised in phase, twice independently, and overlapped to provide a Gaussian random signal which is output by DMA.

Data for display are processed by the DISPLAY INTERFACE. This module receives data from two sources: the array processor, which provides co-ordinates of the analysis data, and the controller, which provides the annotation data. The display interface converts both types of data into patterns suitable for display and holds these in the 'full bit' store, where they are used to drive the CRT.

A hard copy of the displayed data may be obtained either from the video output, for video printers, or from the PLOTTER INTERFACE, for digital or analogue X, Y plotters.

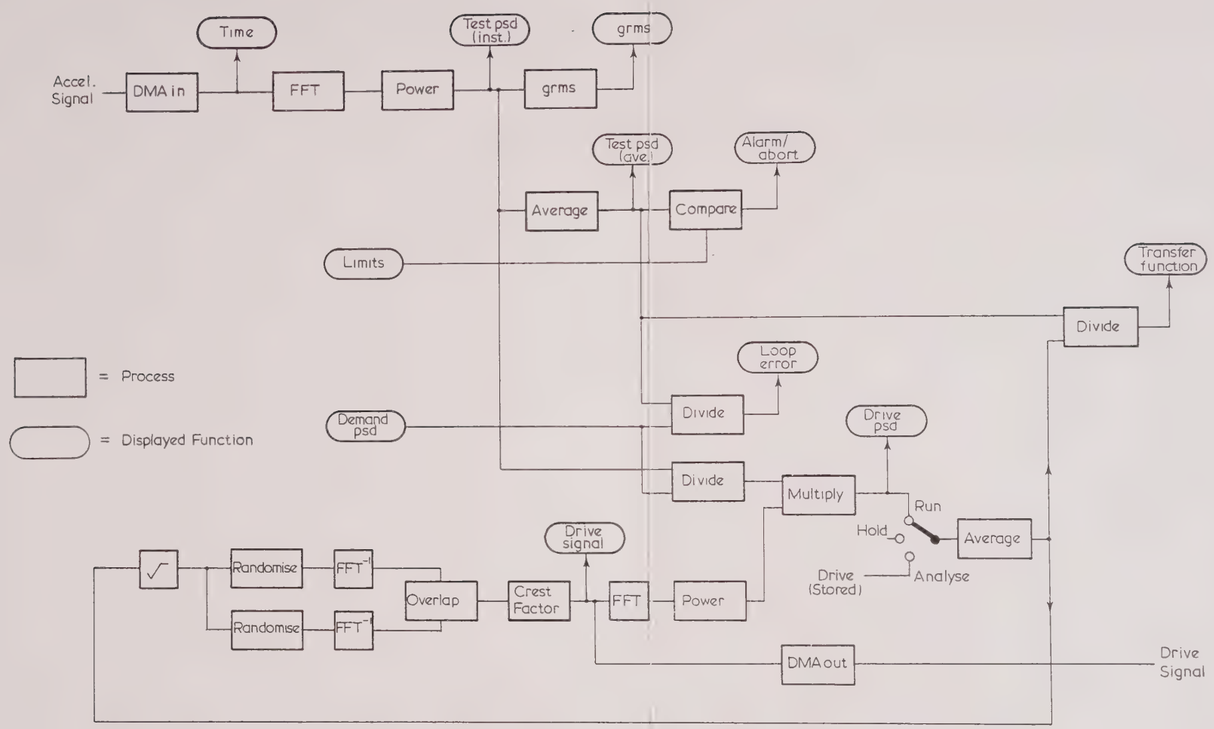

Fig 6.2 Data Processing

Data output to a remotely controlling device are read from the data store by the GPIB interface.

CHAPTER 7

RVC BUS OPERATION

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7. RVC BUS OPERATION

7.1 INTRODUCTION

The RVC is composed of operational 'modules', each of which has a specific task in the overall data flow. Communication between these modules takes place on the RVC bus. A block diagram of this arrangement is shown in Fig 7.1

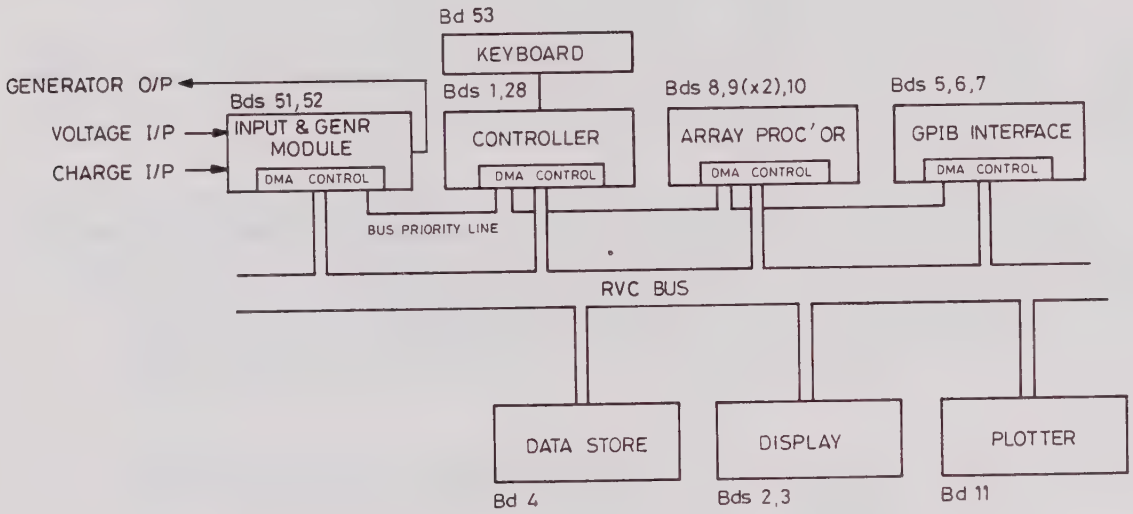

Fig 7.1 RVC operational modules

To save time in managing the large amount of data used in signal processing, data are transferred directly from module to module by the use of direct memory access (DMA). As shown in Fig 7.1, four modules are capable of controlling DMA data transfers and these modules share the use of the RVC bus in accordance with a fixed priority dependent on a module's position in a hardwired priority line.

When a module is in control of the bus it is known as the bus 'master'. The bus master can address one other module, known as the 'slave', and can write data to it or read data from it, via the module's data 'registers'.

Supervisory control of the data flow is achieved by the controller module, in accordance with its internal program. The controller defines the tasks to be performed. When a bus master has completed such a task it alerts the controller by means of a program 'interrupt'.

Details of each of these aspects of RVC bus operation are given in Sub-Sections 7.1 to 7.4 below. Details of the functions of specific data registers are given in Chapter 8.

7.2 BUS MASTERY

An RVC module can obtain bus mastery, i.e. control over the RVC bus functions, only if:

* it is given a task by the controller

* a higher priority module is not requesting bus mastery.

* no other module is using the bus.

To define the task that a module is to perform, the controller, acting as bus master, writes the task definition into the module's control registers. When it has received this information, which includes a 'GO' command, the module requests bus mastery by outputting a BUS REQUEST signal.

Four modules in the RVC are capable of being bus master, therefore a priority structure exists to decide which module should achieve bus mastery in the event of multiple requests. This structure is shown in Fig 7.2. A module can achieve bus mastery only if its bus priority input (BPI) is Lo, signifying that no higher priority module is requesting bus mastery.

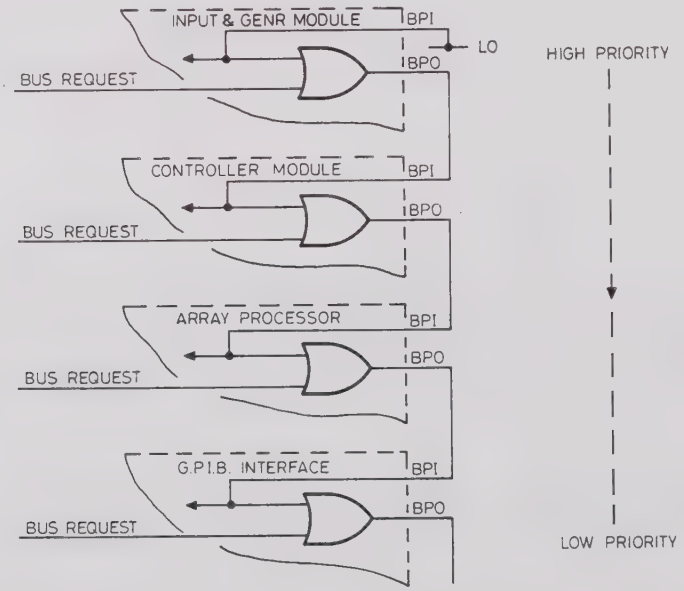

Fig 7.2 Bus request priority structure

No module, whatever is priority, can interrupt a bus cycle. This is ensured by means of the BUSY line, which the current bus master holds Lo for the cycle duration. Before a module can achieve bus mastery, therefore, it must also wait for it's BUSY input to go Hi.

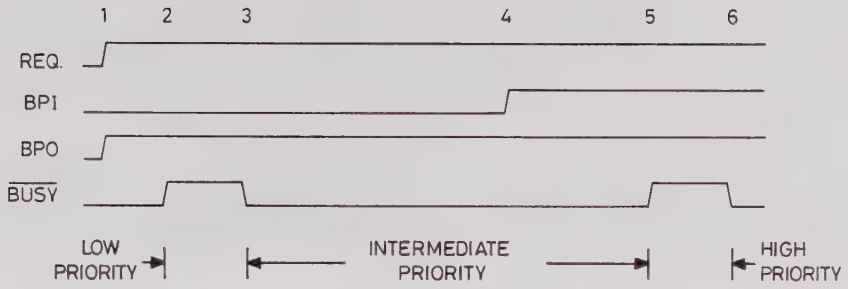

Fig 7.3 Bus mastery transfer timing

The timing of the BUS REQUEST, bus priority and $\overline{\text{BUSY}}$ signals during a typical bus mastery transfer is shown in Fig 7.3. The sequence is a follows:

1. An intermediate priority module, e.g. the array processor, requests bus mastery whilst a lower priority module, e.g. the GPIB Interface, is using the bus. Note that the input and generator and controller modules have allowed the BPI of the array processor to go Lo (= bus not wanted).

2. The GPIB interface, having completed the current bus cycle, takes the $\overline{\text{BUSY}}$ line Hi to signify 'bus free'.

3. The array processor assumes bus mastery and takes the $\overline{\text{BUSY}}$ line Lo to signify 'bus busy'.

4. The input and generator module requests bus mastery, hence taking Hi the BPI of the array processor.

5. The array processor, having completed the current bus cycle, takes the $\overline{\text{BUSY}}$ line Hi.

6. The input and generator module assumes bus mastery and takes the $\overline{\text{BUSY}}$ line Lo again.

7.3 DATA TRANSFERS

Data transfers on the RVC bus take place on a 16 bit data highway, between the bus master and one other module known as the slave. These transfers are controlled by the bus master, which can either write data to the slave or read data from it. Access to the slave is obtained via data or control registers, which the bus master addresses via a 16 bit address highway.

The bus signals that are used to control a data transfer are $\overline{\text{WRITE}}$, $\overline{\text{READ}}$, and $\overline{\text{ACK}}$. The significance and timing of these signals during a write transfer and a read transfer is now explained, with reference to Figs. 7.4 and 7.5.

7.3.1 Write Sequence

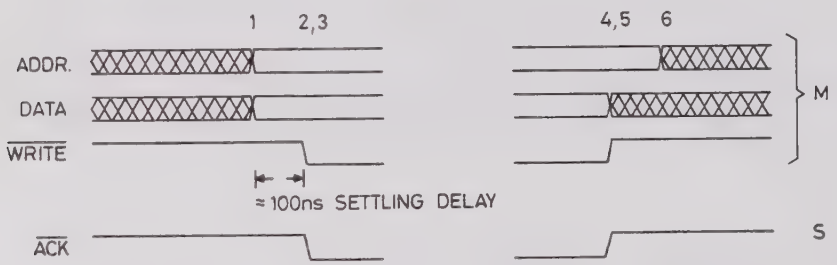

Fig 7.4 Write sequence timing

1. The bus master outputs the address of the register involved in the transfer and the data to be written into it.

2. The bus master takes the $\overline{\text{WRITE}}$ line Lo, to tell the slave that the data is ready.

3. The slave takes the $\overline{\text{ACK}}$ (acknowledge bar) line Lo, to signify 'data received'.

4. The master negates the $\overline{\text{WRITE}}$ signal.

5. The slave takes the $\overline{\text{ACK}}$ line Hi, to acknowledge the completion of the data transfer.

6. The master removes the address and data from the bus.

7.3.2 Read Sequence

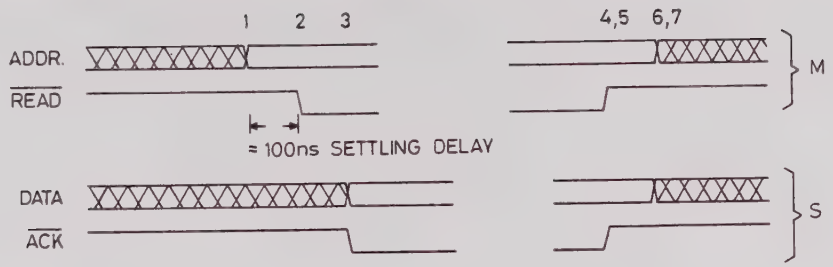

Fig 7.5 Read Sequence Timing

1. The bus master outputs the address of the register to be read.

2. The master takes the $\overline{\text{READ}}$ line Lo, to tell the slave to gate the register outputs onto the bus.

3. The slave complies, and takes the $\overline{\text{ACK}}$ line Lo to show that it has done so.

4. The master reads the register contents, then takes the $\overline{\text{READ}}$ line Hi to indicate 'data received'.

5. The slave takes the $\overline{\text{ACK}}$ line Hi to acknowledge completion of the data transfer.

6. The master removes the address from the bus.

7. The slave removes the data from the bus.

7.4 INTERRUPT REQUESTS

To allow the RVC program to be executed as quickly as possible, the controller does not wait for each module to complete its alloted task before progressing to the next instruction. Instead, having defined the task, it carries straight on, leaving the module to request an interrupt on task completion.

Often, several modules may be requesting an interrupt at the same time. Therefore, each module is allocated a unique position in a time dependent priority structure. When the controller is ready to service an interrupt, it outputs a SYNC pulse to all modules on the RVC bus. Any module needing attention will then output an INT pulse in return, after a delay dependent on the module's particular interrupt priority. As shown in Fig 7.6, fifteen time 'slots', defined by the BCLK signal, are available for outputting an INT pulse; the first slot has the highest priority and the last slot the lowest.

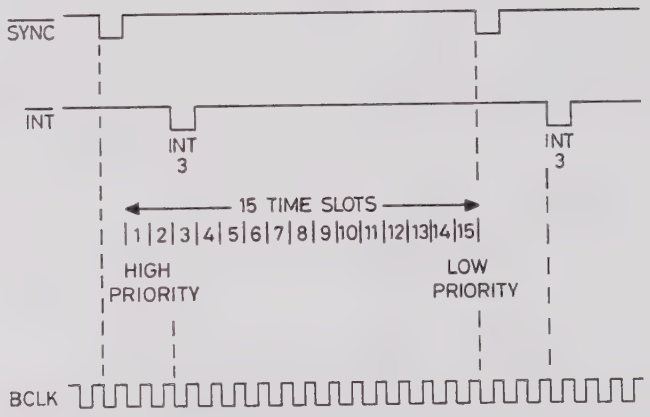

Fig 7.6 Interrupt request priority structure.

7.5 DMA CONTROL

DMA control on each of the four possible bus masters (input and generator module, controller, array processor, and GPIB interface) is implemented by an LSI chip, type PAL16 R4, that is programmed for this purpose at the factory. The way in which this chip operates for the read and write cycles is explained below. Each possible bus master can also be a slave and the PAL16 R4 chip contains the logic for this. The slave logic in the remainder of the RVC modules is composed of discrete logic elements and, in some cases, the timing varies slightly from that of the slave logic in the PAL16 R4 chip. The effect of the signals, however, is exactly the same.

7.5.1 Read Cycle

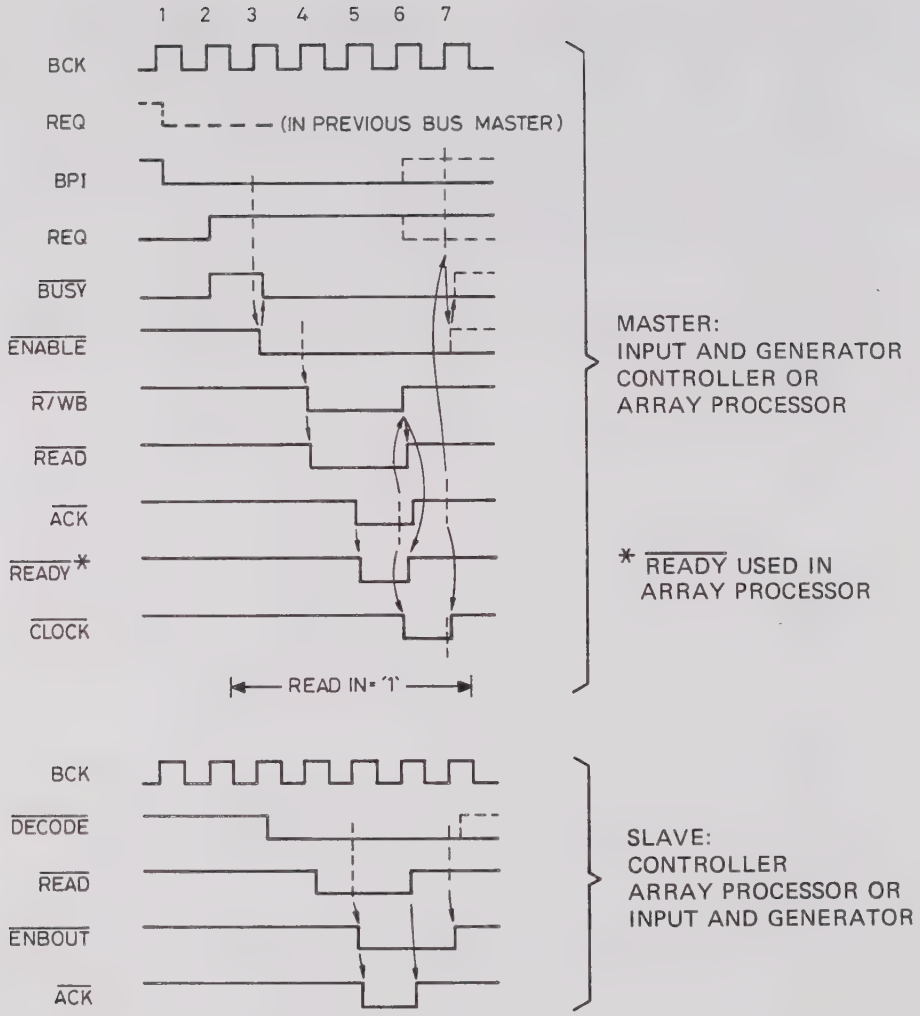

Fig 7.7 Read Cycle

The basic read cycle is shown in Fig 7.7. For all signals except BPI, REQ and BUSY the timing is always the same. The timing of BPI, REQ and BUSY can vary considerably, although, for a read cycle to occur, these signals must be in the states Lo, Hi and Hi respectively when the positive going edge of BCK(3) occurs. The basic read cycle applies to the following master-slave relations:

Master	Slave
Input and generator Module	Controller or Array Processor
Controller	Input and generator Module or Array Processor
Array Processor	Input and generator Module or Controller

The events that occur prior to and during the read cycle are as follows:

1. In the previous, higher priority, bus master, the REQUEST signal is cleared on the positive going edge of BCK and causes the bus priority input (BPI) of the present module to go Hi (= bus available).

2. The present module claims the bus by taking the REQuest line Hi and the previous bus master relinquishes the bus by taking the $\overline{\text{BUSY}}$ line Hi. (These two events do not necessarily occur at the same time).

3. The signal decode BPI=Lo, REQ=Hi and $\overline{\text{BUSY}}$=Hi allows $\overline{\text{ENABLE}}$ to be clocked Lo; this enables the present module to output the address of the 'slave'. $\overline{\text{ENABLE}}$, in going Lo, takes $\overline{\text{BUSY}}$ Lo also, to secure the use of the bus.

   The signal decode $\overline{\text{ENABLE}}$ = Lo, $\overline{\text{ACK}}$ = Hi and $\overline{\text{CLOCK}}$ = Hi allows R/$\overline{\text{WB}}$ to be clocked Lo. This, in combination with READ IN = '1' (Hi), produces a Lo $\overline{\text{READ}}$ command for the slave.

4. In the slave, the Lo $\overline{\text{READ}}$ signal, in combination with a Lo $\overline{\text{DECODE}}$ signal produced by the address, and a Hi $\overline{\text{ENABLE}}$ signal, allows $\overline{\text{ENBOUT}}$ to be clocked Lo. This enables the slave to place the contents of its output data latches on the bus. $\overline{\text{ENBOUT}}$ = Lo, in combination with $\overline{\text{READ}}$ = Lo and $\overline{\text{DECODE}}$ = Lo, takes $\overline{\text{ACK}}$ Lo also, thus signalling to the master that data is available.

5. In the master, the Lo $\overline{\text{ACK}}$ signal causes the data from the slave to be stored in the input data latches. In the case of the array processor being bus master, $\overline{\text{ACK}}$ is decoded in combination with $\overline{\text{ENABLE}}$ = Lo, R/$\overline{\text{WB}}$ = Lo and READIN = Hi to produce a Lo $\overline{\text{READY}}$ signal, and this is used to clock the data into the input data latches.

6. In the master, the first positive going edge of BCK that occurs after $\overline{\text{ACK}}$ goes Lo prepares the master for the next bus cycle. R/$\overline{\text{WB}}$ is clocked Hi and clears $\overline{\text{READ}}$ and $\overline{\text{READY}}$. $\overline{\text{CLOCK}}$ is clocked Lo and is used to set up the cycle parameters. In the slave, $\overline{\text{READ}}$ returning Hi clears $\overline{\text{ACK}}$.

7. In the master, the signal decode $\overline{\text{ENABLE}}$ = Lo, $\overline{\text{CLOCK}}$ = Lo and $\overline{\text{ACK}}$ = Hi allows the states of BPI and REQ to be checked. If BPI = Lo (bus not wanted by higher priority module) and REQ = Hi (bus wanted by present bus master) then $\overline{\text{ENABLE}}$ AND $\overline{\text{BUSY}}$ remain Lo and the present module begins another bus cycle; if not, then $\overline{\text{ENABLE}}$ and $\overline{\text{BUSY}}$ are cleared and the module relinquishes bus mastery until the signal combination BPI = Lo, REQ = Hi and $\overline{\text{BUSY}}$ = Hi occurs again.

   In the slave, the Hi state of the $\overline{\text{READ}}$ signal allows $\overline{\text{ENBOUT}}$ to be clocked Hi to remove the contents of the output data latches from the bus.

7.5.2 Read Cycle with $\overline{\text{HOLD}}$

The $\overline{\text{HOLD}}$ signal is used by the GPIB interface, when this module is acting as bus master in control of a read cycle. The effect of HOLD is to delay the resetting of R/$\overline{\text{WB}}$ by ACK, as shown in Fig 7.8. This delay allows the GPIB interface time to load the data into its input latches. The sequence of events is the same as that of the basic read cycle, except that the resetting of R/$\overline{\text{WB}}$ and the events following it occur one BCK period later.

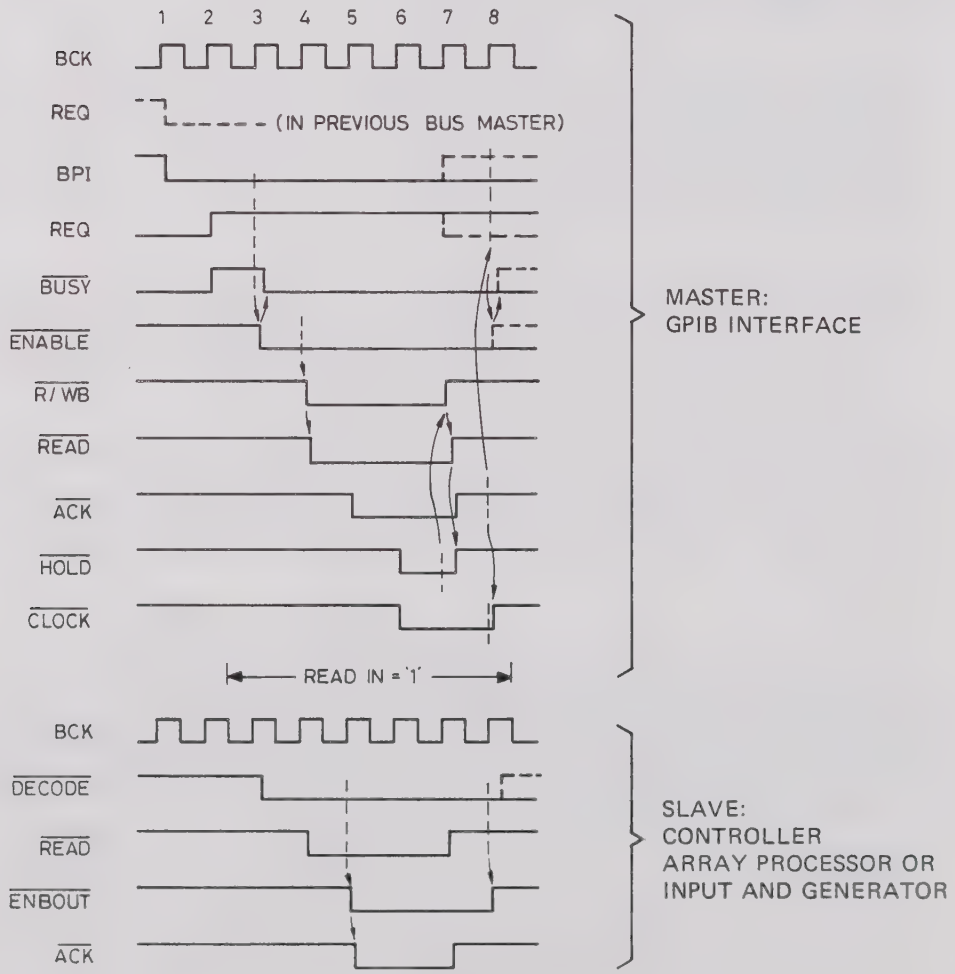

Fig 7.8 Read Cycle with Hold

7.5.3 Read Cycle with Acknowledge INHibit

The ACK INH signal is used by the GPIB Interface, when this module is acting as the slave in a read cycle. The effect of ACK INH is to delay the ACK signal and thus allow the GPIB Interface time to load the data into its output latches. As shown in Fig 7.9, the sequence of events is the same as that of the basic read cycle, except that ACK and the events following it occur one BCK period later.

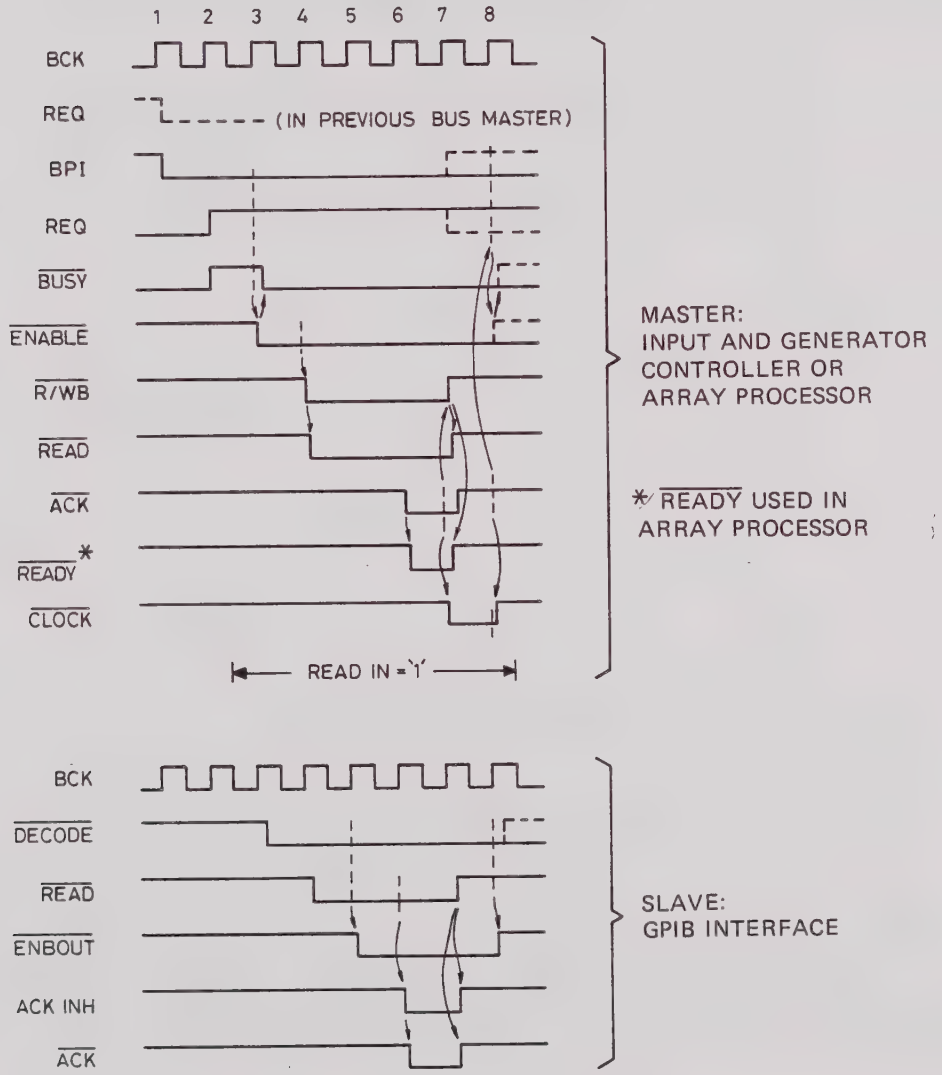

Fig 7.9 Read cycle with ACKnowledge INHibit

7.5.4 Write Cycle

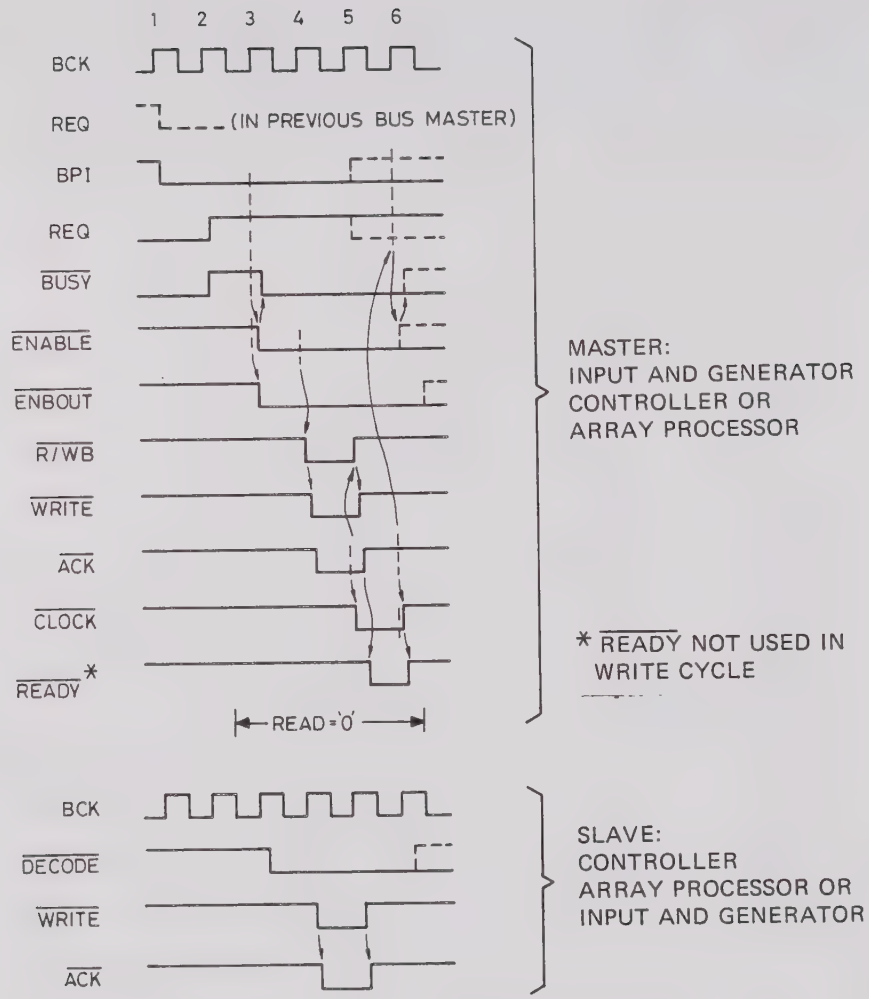

Fig 7.10 Write Cycle

The basic write cycle is shown in Fig 7.10. For all signals except BPI, REQ and BUSY the timing is always the same. The timing of BPI, REQ and BUSY can vary considerably, although, for a write cycle to occur, these signals must be in the states Lo, Hi and Hi respectively when the positive going edge of BCK(3) occurs. The basic write cycle applies to the following master-slave relations:

Master	Slave
Input and generator Module	Controller or Array Processor
Controller	Input and generator Module or Array Processor
Array Processor	Input and generator Module or Controller
GPIB Interface	Input and generator Module, Controller or Array Processor

The events that occur prior to and during the write cycle are as follows:

1. In the previous, higher priority, bus master, the REQUEST signal is cleared on the positive going edge of BCK and causes the bus priority input (BPI) of the present module to go Hi (= bus available).

2. The present module claims the bus by taking its request output Hi and the previous bus master relinquishes the bus by taking the BUSY line Hi. (These two events do not necessarily occur at the same time).

3. The signal decode BPI=Lo, REQ=Hi , $\overline{\text{ENABLE}}$ = Hi, $\overline{\text{BUSY}}$ = Hi and READIN = Lo allows ENABLE to be clocked Lo; thus enabling the master to output the address of the slave. ENABLE, in going Lo, takes the BUSY line Lo also, to secure the use of the bus.

   $\overline{\text{ENBOUT}}$ is maintained Lo during the write cycle by the decode $\overline{\text{ENABLE}}$ = Lo and READIN = Lo.

4. The signal decode $\overline{\text{ENABLE}}$ = Lo, $\overline{\text{ACK}}$ = Hi and $\overline{\text{CLOCK}}$ = Hi allows R/WB to be clocked Lo. This, in conjunction with READIN = '0' (Lo), produces a Lo WRITE command for the slave.

   In the slave, the Lo $\overline{\text{WRITE}}$ command, in combination with a Lo $\overline{\text{DECODE}}$ signal produced by the address, enables the data output from the master to be stored in the slave's input latches. The $\overline{\text{WRITE}}$, $\overline{\text{DECODE}}$ combination also produces a Lo ACK signal to tell the master that the data has been received.

5. In the master, the first positive going edge of BCK that occurs after ACK goes Lo prepares the master for the next bus cycle. R/WB is clocked Hi and clears WRITE. $\overline{\text{CLOCK}}$ is clocked Lo and is used to set up the cycle parameters.

   In the slave, $\overline{\text{WRITE}}$ returning Hi clears $\overline{\text{ACK}}$.

6. In the master, the signal decode $\overline{\text{ENABLE}}$ = Lo, $\overline{\text{CLOCK}}$ = Lo and $\overline{\text{ACK}}$ = Hi allows the states of BPI and REQ to be checked. If BPI = Lo (bus not wanted by high priority module) and REQ = Hi (bus wanted by present module) then ENABLE and BUSY remain Lo and the present module begins another bus cycle; if not, then ENABLE and BUSY are cleared and the module relinquishes bus mastery until the signal combination BPI = Lo, REQ = Hi and BUSY = Hi occurs again.

7.5.5 Write Cycle with ACKnowledge INHibit

The ACK INH signal is used by the GPIB Interface when this module is acting as the slave in a write cycle. The effect of ACK INH is to delay the ACK signal until the GPIB has loaded the data into its input latches. As shown in Fig 7.11 the sequence of events is the same as that of the basic write cycle, except that ACK and the events following it occur two BCK periods later.

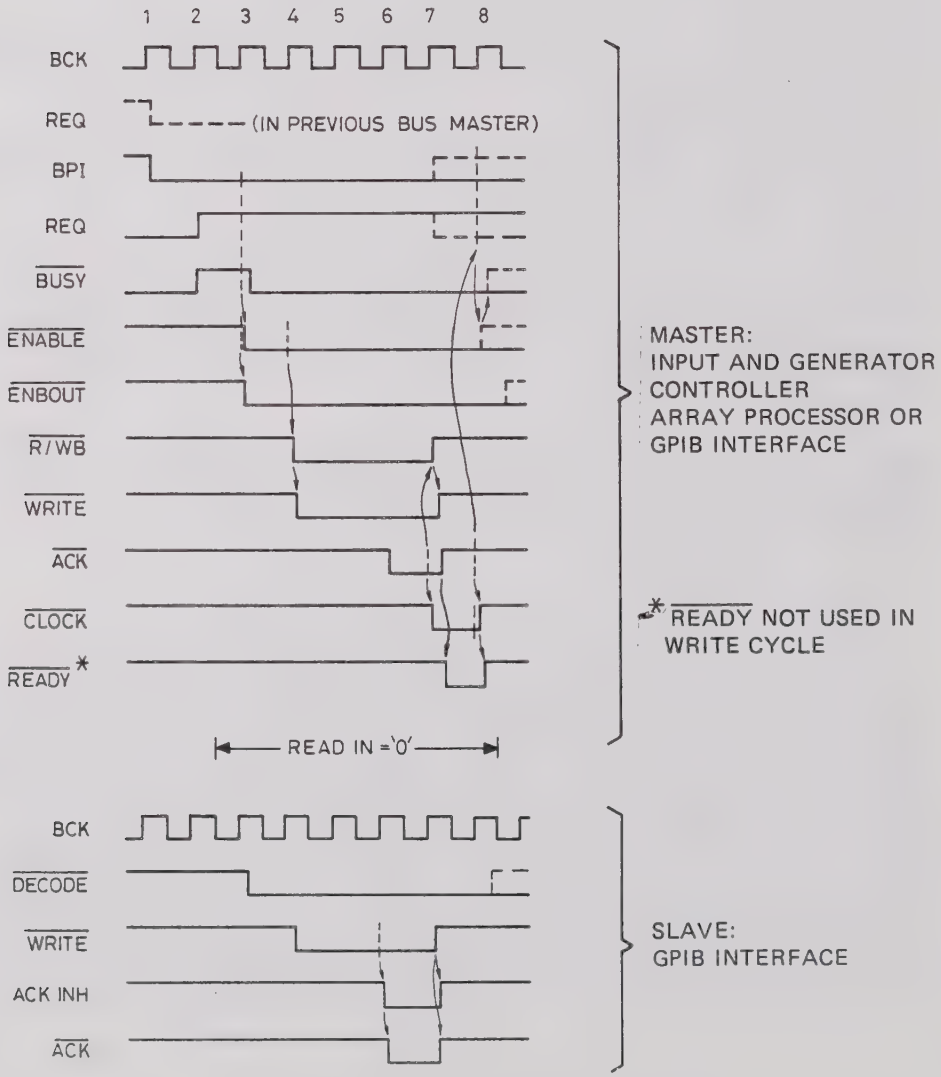

Fig 7.11 Write cycle with ACKnowledge INHibit

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SECTION 8.1 INPUT AND GENERATOR MODULE

The input and generator sections of the RVC are contained in a single module, which comprises boards 51 and 52. Board 52 contains the signal processing circuitry, whilst board 51 contains the DMA control logic.

8.1.1 Input

The input section converts an analogue signal, applied to the voltage or charge input of the RVC, into the digital form required for analysis.

A block diagram of the input section is shown in Fig 8.1. The circuitry appears on sheets 1 to 3 of Circuit Diagram 12107552.

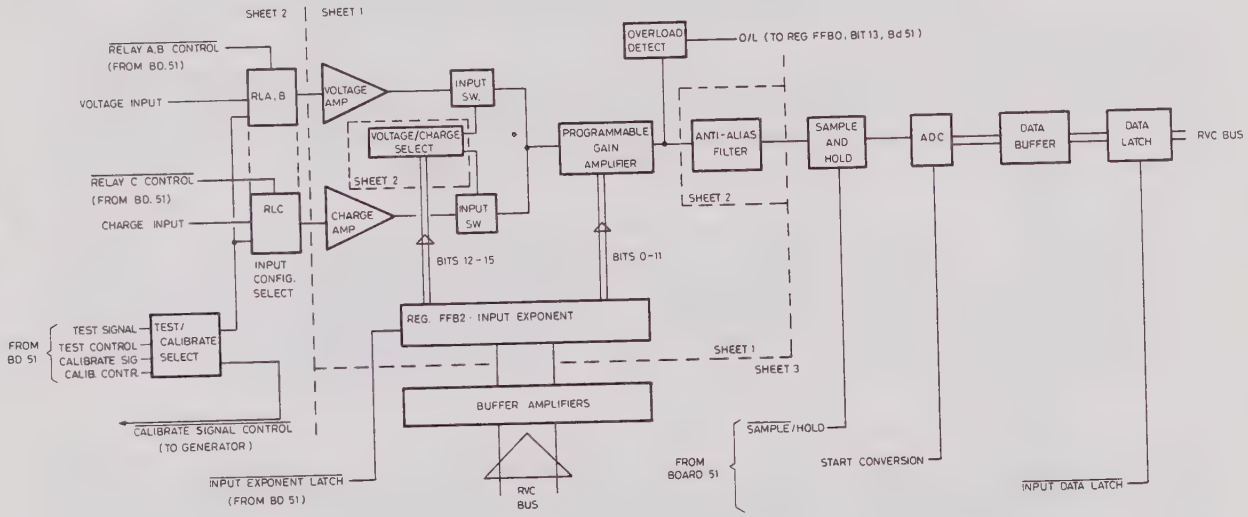


Fig 8.1 RVC input section.

Control over the initial input stages is exercised through registers FFB1 and FFB2. The first of these is located on board 51 (DMA control), whilst the second is on board 52. Register FFB2 has written into it the measurement value exponent; bits 15 to 12 of this are used to select either the voltage or the charge input stage, whilst bits 11 to 0 define an amplification factor for the programmable gain amplifier. Register FFB1 contains the relay and calibrate control data that define the signal to be applied to the selected input stage: the test signal, the calibrate signal, or the signal to be analysed. A description of register FFB1 is given in Section 8.1.3.

The data used in register FFB2 are listed in Tables 8.1 and 8.2.

Table 8.1 Function of Register FFB2, Bits 15 to 12

Bits	15	14	13	12	Input Selected
	0	0	0	0	Voltage
	0	0	0	1	Charge

Table 8.2 Function of Register FFB2, Bits 11 to 0

Bits 11	10	9	8	7	6	5	4	3	2	1	0	Range Selected
0	0	0	0	0	1	0	0	0	0	0	1	10V
0	0	0	0	0	1	0	0	0	0	1	0	5V
0	0	0	0	1	0	0	0	0	0	1	0	2.5V
0	0	0	0	1	0	0	0	0	1	0	0	1.2V
0	0	0	1	0	0	0	0	0	1	0	0	0.63V
0	0	0	1	0	0	0	0	1	0	0	0	0.31V
0	0	1	0	0	0	0	0	1	0	0	0	0.16V
0	0	1	0	0	0	0	1	0	0	0	0	0.08V
0	1	0	0	0	0	0	1	0	0	0	0	0.04V
0	1	0	0	0	0	1	0	0	0	0	0	0.02V
1	0	0	0	0	0	1	0	0	0	0	0	0.01V

The programmable gain amplifier is set to produce a maximum voltage swing of ±10V at the input of the ADC. On auto ranging the output of the overload detector is monitored by the System Controller and the range value set into register FFB2 is updated until the detector indicates that an overload is no longer present.

An anti-alias filter attenuates all input signal frequencies >3kHz. Sample and hold then converts the band limited signal into discrete samples and each of these is converted by the ADC into 2s complement binary to be stored in the measurement data latch. The transference of data from the latch to buffer memory is controlled on board 51, as described in Section 8.1.3.

8.1.2 Generator

The generator converts digital signal data, obtained from the RVC memory, into the analogue form required for stimulating the system under test or calibrating the input section of the RVC.

A block diagram of the generator is shown in Fig 8.2. The circuitry appears on sheets 4 and 5 of Circuit Diagram 12107552.

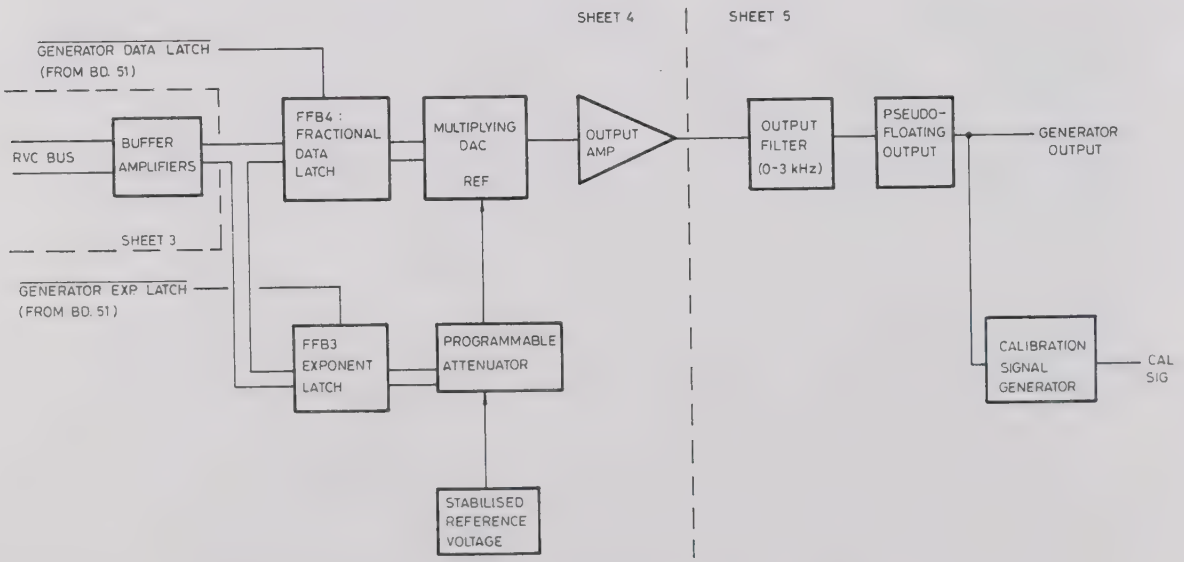


Fig 8.2 RVC generator.

The digital signal data are arranged in blocks, each of which consists of an exponent and 840 fractional values. The exponent, which defines the signal amplitude is stored in register FFB3. Here it is used, via a variable attenuator, to control the magnitude of the stabilised voltage applied to the reference input of a 16-bit multiplying DAC. The exponent values used and the associated signal amplitudes are listed in Table 8.3. Each fractional value is latched in turn in register FFB4, and from this it is applied to the DAC data input. The rate at which the fractional values are latched is determined by the frequency of the sample clock; the sample clock frequency thus determines the frequency content of the generator output signal. Control over the sample clock frequency is exercised through register FFB6, as described in Section 8.1.3.

Table 8.3 Generator Output Signal Amplitudes

Bits	15	14	13	12	11	10	9	8	7	6	5	4	Amplitude Selected
	1	0	0	0	0	0	1	0	0	0	0	0	10V
	0	1	0	0	0	0	1	0	0	0	0	0	5V
	0	1	0	0	0	0	0	1	0	0	0	0	2.5V
	0	0	1	0	0	0	0	1	0	0	0	0	1.2V
	0	0	1	0	0	0	0	0	1	0	0	0	0.63V
	0	0	0	1	0	0	0	0	1	0	0	0	0.31V
	0	0	0	1	0	0	0	0	0	1	0	0	0.16V
	0	0	0	0	1	0	0	0	0	1	0	0	0.08V
	0	0	0	0	1	0	0	0	0	0	1	0	0.04V
	0	0	0	0	0	1	0	0	0	0	1	0	0.02V
	0	0	0	0	0	1	0	0	0	0	0	1	0.01V

To ensure that the correct exponent is applied to the DAC with the first fractional value, register FFB3 is double buffered. The exponent is written into the first buffer to await the first fractional value and, when the first fractional value is written into register FFB4, the exponent is transferred to a second buffer, which acts directly on the variable attenuator.

The amplified output of the DAC is band-limited by passing it through a 0-3kHz filter. Thus the stimulus signal applied to the system under test contains only those frequencies covered by the RVC analysis.

A pseudo-floating output stage ensures that any external voltage fed back to the generator appears equally on the Hi and the Lo output connectors, thus allowing the connectors to 'float' at the external voltage whilst maintaining the generator output voltage between them. This is achieved by a special cross-feedback configuration.

8.1.3 DMA Control

Data received from the input section and data to be output to the generator are held in a cyclic buffer in the RVC memory. The buffer has a capacity of three data blocks, and each block contains an input exponent, a generator exponent, and 1680 input-generator data word pairs, arranged as shown in Fig 8.3. Data transfers to and from the buffer are controlled by the DMA logic on board 51.

A block diagram of the DMA logic is shown in Fig 8.4, whilst the circuitry appears on Circuit Diagram 12107551, sheets 1-3.

Address		
0	input exponent	
1	generator exponent	
3	input data (1)	
4	generator data (1)	
5	input data (2)	Data Block 1
6	generator data (2)	
etc.		
to		
3360	input data (1680)	
3361	generator data (1680)	
3362	input exponent	
3363	generator exponent	
3364	input data (1)	
3365	generator data (1)	Data Block 2
etc.		

Fig 8.3 DMA data format.

The registers involved in input and generator data transfers are:

			Location
FFB0	DMA Control register	(R/W)	Board 51
FFB1	Relay/calibrate control	(W)	"
FFB2	Input exponent	(W)	Board 52
FFB3	Generator exponent	(W)	"
FFB4	Generator data	(W)	"
FFB6	Sample frequency	(W)	Board 51
FFB7	Block word count	(W)	"
FFB8	DMA address control	(W)	"
FFB9	DMA address control	(R)	"
FFBA	DMA word count	(R)	"
FFBB	DMA address count	(R)	"
FFBC	DMA re-initialise	(W)	"
FFBD	DMA load address	(W)	"
FFBE	DMA load word count	(W)	"
FFBF	DMA enable	(W)	"

'Start', 'stop' and 'abort' control of the input and generator sections is achieved through register FFBO (DMA control). DMA interrupt enable and the overload detect are also serviced through this register, and the register bit assignments are as follows:

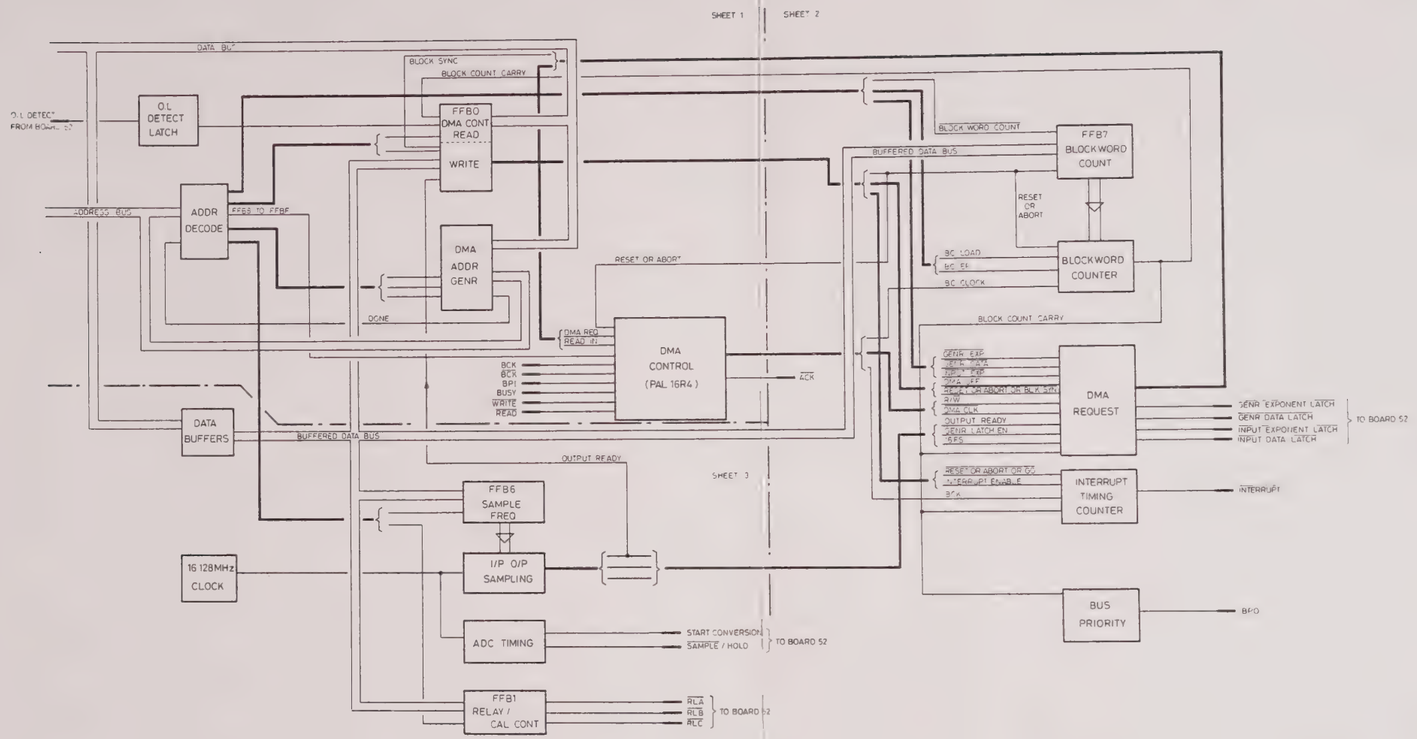


Fig 8.4 DMA Control Logic

Bit	Function
0	DMA 'go'
1	
2	DMA 'off' (R/W)
3	
4	
5	
6	DMA interrupt enable (R/W)
7	
8	Abort (W)
13	Overload detect (R)

Starting from the initialised state, with the DMA 'go' bit set, the DMA control logic accesses locations 0 and 1 of the RVC memory and writes the input exponent and generator exponent values held there into registers FFB2 and FFB3 respectively. This occurs when an 'output ready' signal is produced by the sample clock generator. The frequency of the sample clock is determined by the value written into register FFB6 by the System Controller. As each successive output ready signal occurs the DMA control logic accesses the appropriate locations in memory and transfers an input data word from the input data latch to the buffer and a generator data word from the buffer to the generator data latch. The timing for this is shown in Fig 8.5, which covers the change-over point between the completion of one block and the start of the next.

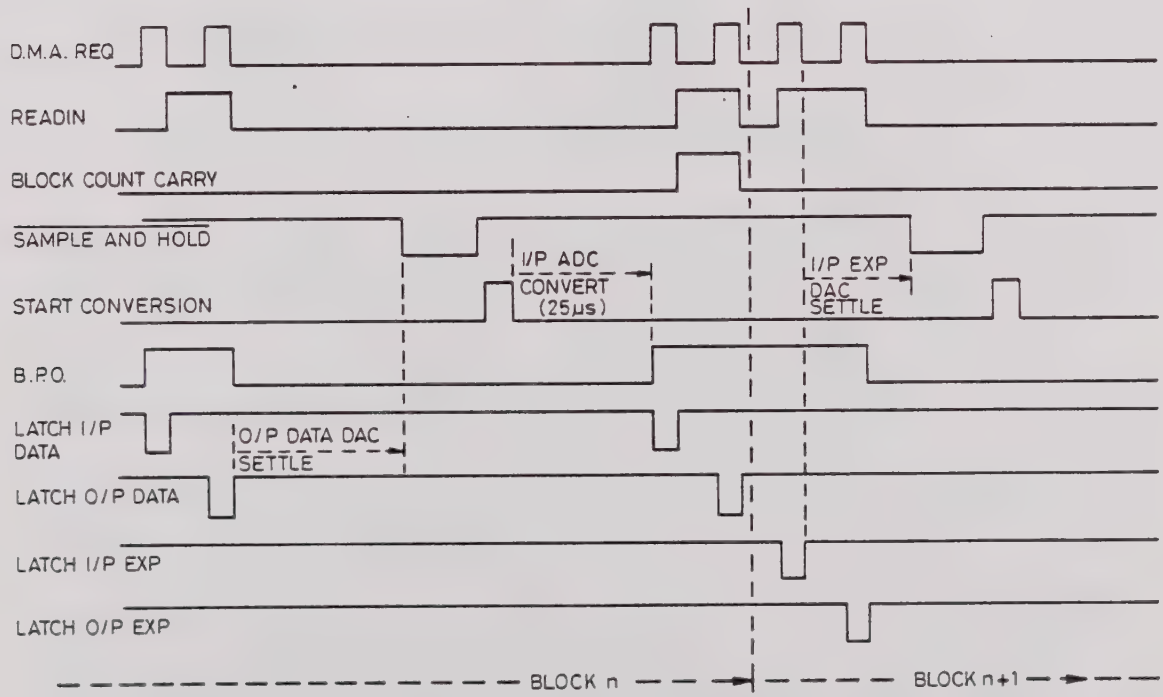


Fig 8.5 Data transfer timing.

Buffer addressing is achieved by the address generator, which is controlled through registers FFB8 to FFBF. This comprises two AM 2940 ICs, which are set to operate in 'Mode 1' by writing 'F9F9' into the DMA control register FFB8. In Mode 1 the memory addresses generated cover the number of words written

into register FFBE (DMA load word count), ranging from the start address loaded into register FFBD (DMA load address).

A count of the number of words transferred within a data block is held in the block word counter. This is loaded, on re-initialisation and on block count carry, with the block word count written into register FFB7. The block word count is in 2s complement form; this allows it to be incremented by the number of words required before producing a carry. When the carry occurs the block word counter is reloaded. Also, if the interrupt enable bit (bit 6 in register FFB0) is set, the DMA control logic interrupts the System Controller. The controller may then process the input data, and update the input and generator exponents and generator data as necessary.

All the DMA counters are incremented by the block count clock, which is generated at the end of each write cycle. When the DMA word count (contained in register FFBA) plus one equals the load word count the address generator issues a Hi 'done' signal. This is used to 're-initialise' the address generator to the start address. The address generator can also be re-initialised by writing a dummy word to register FFBC (DMA initialise); this is normally done at the beginning of a DMA operation.

Register FFB1 contains the relay and calibrate control data that define the signal to be applied to the selected input stage: the test signal, the calibrate signal, or the signal to be analysed. The bit assignments of register FFB1 are:

Bit 0	RLA control; selects signal applied to voltage amplifier '-' input 1 = voltage Hi signal, 0 = test/calibrate signal.
Bit 1	RLB control; selects signal applied to voltage amplifier '+' input 1 = ground potential (0V), 0 = voltage Lo signal.
Bit 2	RLC control; selects signal applied to charge amplifier '-' input 1 = charge signal, 0 = test/calibrate signal.
Bit 3	Test signal control (not implemented)
Bit 4	Calibrate signal control for voltage and current amplifiers 1 = calibrate input grounded 0 = calibrate signal active

SECTION 8.2 CONTROLLER

8.2.1 INTRODUCTION

The controller receives commands from the keyboard interface and GPIB and issues commands to the I/O system, the array processor and the display. These commands are synchronised by interrupts which are serviced by the controller.

The controller is contained on board 1, with the exception of the system software contained in PROM on board 28.

8.2.2 PROCESSOR

The controller is built around a TMS9900 microprocessor (IC14) which is driven by a clock generator (IC39). The clock generator also drives the RVC bus clock and the RVC bus time-out delay, and, after division of the output frequency to 20Hz by IC13, drives the real-time clock and the watchdog.

The processor controls the RVC system via a 16 bit data bus and a 16 bit address bus. A map of the processor address space is given in Table 8.4.

Table 8.4 Processor Address Map

Address Range	Function
0-17FE	Scratch RAM
1800-1FFE	Unused
2000-2FFE	RVC bus window
3000-3FFE	On-board registers
4000-5FFE	Diagnostic Program (S-Bug)
6000-6FFE	Overlay Area
7000-FFFE	Program Root Section

The addresses refer to bytes, but, since the 9900 works on 16 bit data, only even addresses exist. The program is too large to fit into the 64k byte address space, so only a small 'root' section is always addressable, the remainder being overlaid into a 4k byte shared area. There are 16 overlays, which are called up by the value written into a register at 3FF0. The program is arranged to call up the overlays, as required, during normal operation.

8.2.3 RVC BUS INTERFACE

The RVC bus interface is controlled by a PAL16R4 (IC47) as described in Chapter 7. When the controller is bus master it drives the RVC bus address highway, through IC48 and IC49.

The RVC bus covers an address space of 64k words, but only 4k bytes of this can be accessed by the controller at any one time. The actual address range available through the RVC bus window is controlled by a base address written to a mapping register at address 3FFE. The

mapping procedure is further complicated by the conversion of word addresses on the RVC bus to byte addresses on the controller board. The following example should clarify this.

To access the array processor FIFO at RVC bus address FFFB, the controller writes F800 to the mapping register. This maps the 2K words (4K bytes) from F800 - FFFF into the window area (2000 - 2FFE). The FIFO address offset is FFFB - F800 = 7FB words = FF6 bytes. Thus the controller sees the FIFO at 2000 + FF6 = address 2FF6.

8.2.4 BUS TIME-OUT

In case a fault prevents a module on the RVC bus from replying when addressed as a slave in a bus transfer, the controller board contains a time-out circuit (IC19). When READ or WRITE is asserted, IC19 is set. If the bus cycle proceeds normally, READ or WRITE is removed by ACK. Under a fault condition, however, READ or WRITE will still be low after 2.5µs, thus causing the output of IC62 (pin 11) to go low. This provides an ACK signal through IC35 to complete the cycle.

Of course, a cycle terminated by a bus time-out will not normally result in a correct data transfer, but the system will not be held up. To alert the engineer of such a fault, an led (D2) is illuminated if a time-out occurs. The led can be extinguished only by activation of a toggle switch (S3) on the controller board.

Since the led is on after a power-up, the switch must be toggled to clear the indication before checking for a time-out fault.

8.2.5 WATCHDOG

The watchdog consists of a counter (IC2), clocked at the 20Hz rate, whose carry is connected to the restart circuitry. Thus, if the counter reaches its carry state, the processor is restarted.

Normally, the controller software is assigned to write to the watchdog at regular intervals to prevent the carry state being reached, but under fault conditions, which might stop the program executing correctly, the system will be booted by the watchdog.

The time delay between writing to the watchdog and the restart is the reverse of the code written (in 50ms units). Writing 0 to the watchdog, for example, gives a delay of 750ms, while F causes an immediate restart.

The watchdog may be disabled by setting switch S2 on board 1 to 'OFF'. Then, if a spurious restart occurs (power-up sequence executed), the watchdog should be suspected. Disabling the watchdog causes the system to stop when a fault occurs, thus allowing the fault to be investigated.

8.2.6 BOOT PROMS

The controller board contains two PROMS (IC6 and IC8) which contain the boot vector. This consists of a workspace address located at FFFC and a restart address located at FFFE. The boot vector enables the controller to be started without board 28 present, which is a useful aid when diagnosing faults on board 28.

8.2.7 INTERRUPT HANDLING

All RVC bus interrupts (see Chapter 7) are routed to the Controller for service. A counter, IC31, defines the time slots for interrupt multiplexing and generates the SYNC pulse. An interrupt latches the state of the counter into IC32, which provides a decoded value corresponding to the time slot and also generates an interrupt request to the processor.

8.2.8 DIAGNOSTIC SWITCHES

The controller board contains a bank of switches (S1) which can be read by the processor at address 3FF8. The sections of this switch have various functions, as shown in Table 8.5. The default condition for all switches is off.

Table 8.5 Function of Switch S1

Switch Section	Function in ON position
1	Start Diagnostics instead of system program
2	Output keycodes to terminal
3	Disable power-up test
4	Disable error beeper
5	Set generator into calibrate mode
6	Disable interlock
7	Unused
8	Unused

8.2.9 SERIAL INTERFACES

Two serial interfaces are provided. One, using UART IC5, communicates with the Keyboard Interface (board 53). The other interface, using UART IC6, is connected to the serial link on the rear panel. This is not used by the system program, but is available for development and diagnostic functions.

SECTION 8.3 ARRAY PROCESSOR

8.3.1 INTRODUCTION

The array processor is the arithmetic 'workhorse' of the RVC and, as such, it does all the arithmetic operations necessary, on time and frequency related arrays of data, to compute the analysis functions and perform the control loop algorithm.

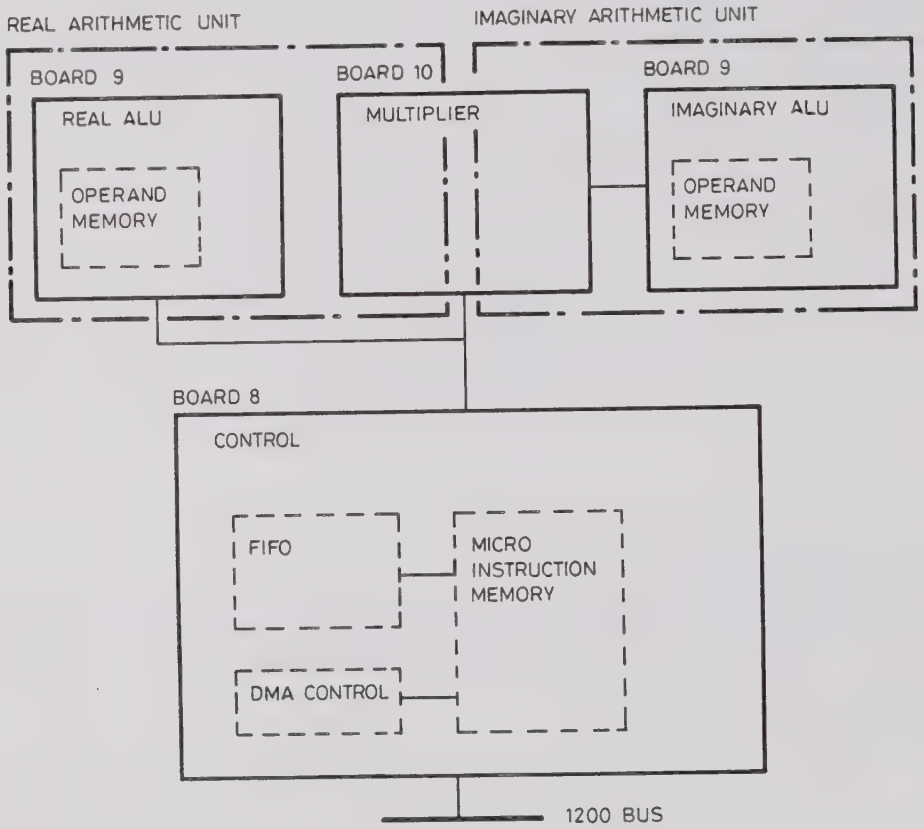


Fig. 8.6 Array processor hardware.

The hardware of the array processor is shown in Fig. 8.6. It comprises two arithmetic units, one for real data and one for imaginary data, and a control unit. The two ALU boards (board 9) are identical and may therefore be 'swapped' over when fault finding at board level. A typical application of this is where a fault on the 'real' ALU has stopped the RVC bus operation; swapping over the two ALUs allows the bus to continue operating, although invalid data will still be obtained.

The two arithmetic units operate in accordance with a series of micro instructions from the array processor control unit. This unit, in turn, operates under the supervision of the system controller.

8.3.2 DATA PROCESSING

The work done by the array processor at any particular time can range from a relative simple task, such as calculating the Fourier transform of a block of time data (into the equivalent frequency data), to a more complex task, such as the computation of the drive signal required to equalise the control loop. Each task, however, consists of a sequence of predefined operations, either for arithmetic or for DMA control. Each operation is executed in accordance with a specific micro instruction routine, identified by a code number that the system controller writes into the array processor FIFO store. A monitor program in the micro instruction memory accesses the FIFO to determine which operations make up the present task. The array processor operations and associated code numbers are listed in Table 8.6.

On power-up or system initialise the monitor program clears the FIFO store and stops. A processing task may then be set up by the system controller, using the FIFO and control registers in the array processor. First, the system controller, acting as bus master, writes a series of operation codes and associated parameters into the FIFO. The controller then writes a GO command into the array processor control register. This causes the micro-instruction monitor program to execute the task, as defined by the FIFO contents, and then to stop. A flow diagram of the monitor program is given in Fig 8.7. Task completion is indicated by the ready bit in the array processor control register or by the ready interrupt.

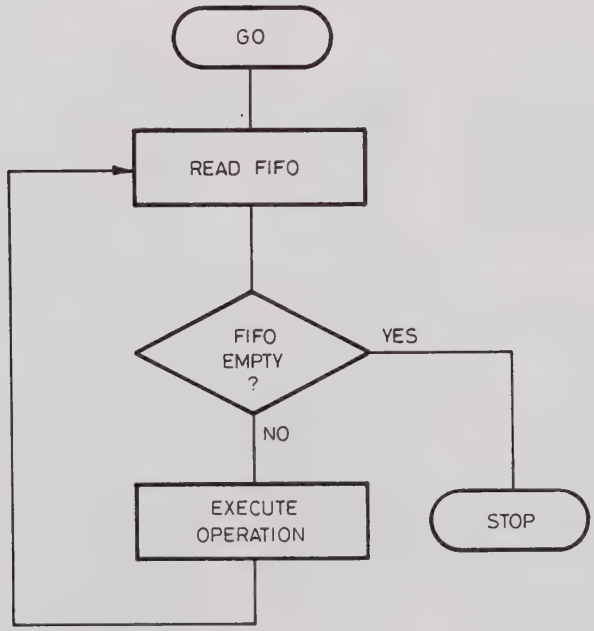


Fig. 8.7 Monitor program flowchart

During task execution, data are transferred into, and out of, the array processor (with this module acting as bus master) via the DATA register. This register accesses the operand memory in the 'real' arithmetic unit. A data link between this memory and its companion in the 'imaginary' arithmetic unit is achieved with 'swap' latches on the multiplier board (board 10). The operand memories contain a 'scratch pad' area and various storage areas, as shown in Fig. 8.8.

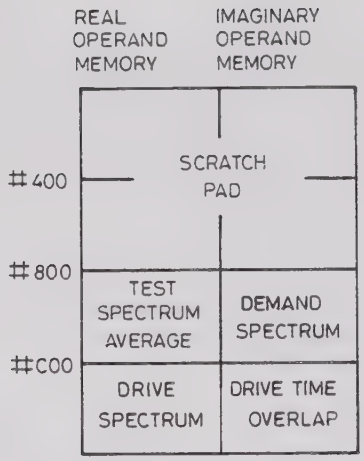


Fig. 8.8 Operand memory map.

Table 8.6 Array Processor Operations

Version 09
Date 11-JUL-83

Num	Command	Arguments	Source	Destination	Description
00	APNOOP				no operation
01	APSTOP				stop ap (debug)
02	APDMIN	be;se;sm			dma initialise
03	APDMIR	n;sa;ma;ea;b	1200 words	ap real	dma in real
04	APDMII	n;sa;ma;ea;b	1200 words	ap imag	dma in imag
05	APDMIC	n;sa;ma;ea;b	1200 words	ap cplx	dma in cplx
06	APDMIS	n;sa;ma;ea;la	1200 alt wrds	ap cplx	dma in skip
07	APDMOR	n;sa;ma;ea;d	ap real	1200 words	dma out real
08	APDMOI	n;sa;ma;ea;d	ap imag	1200 words	dma out imag
09	APDMOC	n;sa;ma;ea;d	ap cplx	1200 words	dma out cplx
0E	AP840I		840 pts cplx	in place (#0)	inverse fft
0F	AP840F		840 pts cplx	in place (#0)	forward fft
11	APFILZ	n;sa;t	zero	ap r/i/c	fill with zero
12	APDSPS	n;sa;fh;fl;o	dp real	dp real	display scaling
13	APR	n;sa	dp cplx	dp real (im=0)	magnitude
14	APLOG	n;sa	dp real	dp real	log (base e)
15	APHANN	n;sa	sp cplx	sp cplx	hanning window
19	APBXMX	n;sea;mea	1200 words	1200 words	find max exp
1A	APSXHX	n;sa;da	dp cplx	dp real (im=0)	power
1B	APTHTA	n;sa	dp cplx	dp real (im=0)	phase
1C	APDMIX	n;sa;ma;ea;b	1200 words	ap cplx dp	dma in extend
1D	APSPDP	n;sa;da;t	sp r/i/c	dp r/i/c	sp -) dp
1E	APDPSP	n;sa;da;t	dp r/i/c	sp r/i/c	dp -) sp
1F	APAVGR	n;sa;aa;ke;km	dp real & avge	dp real avge	average
22	APDMSC	sm	1200 word	ap internal	set dma scaling
23	APSCAL	n;sa;se;sm;t	dp r/i/c	dp r/i/c	scale (*)
24	APOFST	n;sa;oe;om;t	dp r/i/c	dp r/i/c	offset (+)
28	APMOVE	n;sa;ts;da;td	r/i/c	r/i/c	move data
2D	APLIMT	n;sa;la	dp real	1200 words	find max data
2F	APHYST	n;sa;ar	dp real	dp real	hysteresis
3B	APNORM	n;sa;t	dp r/i/c	dp r/i/c	normalise
3E	APSQRT	n;sa	dp real	dp real	square root
40	APTWID	n;sa	sp cplx	sp cplx	fwd twiddle
41	APDMOS	n;sa;ma;ea;d	ap cplx	1200 alt wrds	dma out skip
42	APFRES	n;sa;k	dp real	dp real	freq resolution
43	APTWIN	n;sa	sp cplx	sp cplx	inv twiddle
44	APCOMP	n;sa;ca;la	dp real/sp comp	1200 words	compare
45	APGRMS	n;sa;ma	dp real	1200 words	total power
46	APMULT	n;sar;sac;sap	dp real/imag	dp real	multiply
47	APDIV	n;san;sad;saq	dp real/real	dp real	divide
48	APRAND	n;sa;r0	sp real	sp cplx	randomise phase
49	APEXCH	n;sa;da	cplx	cplx	exchange data

Table 8.6 cont.

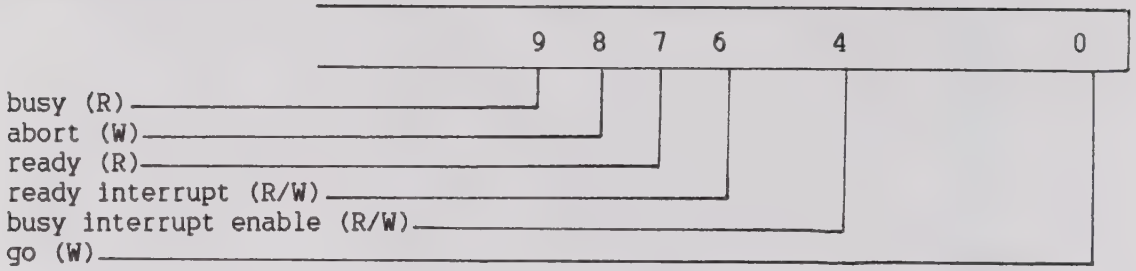
4A	APOVLP	n;sa1;sa2;dsa	sp c/c/i	sp c/i	overlap data
4B	APSNOR	n;sa;t;me	sp r/i/c	sp r/i/c	sp normalise
4C	APFIX	n;sa	dp real	dp real	integerise
4D	APCRST	n;sa;ce;cm	sp cplx	sp cplx	crest factor
4E	APRATE				
4F	APTHRS	n;sa;ra;m;m;t;t	dp real/imag	dp real	threshold
50	APCHCK	n;sa;c;l;se;sm	dp real/real	1200 word	check level
51	APLOCR	n;sa;r0	sp real	sp cplx	Schroeder phase
52	APSOFT	n;sa;ce;cm	sp cplx	sp cplx	soft clipping
53	APFPBE	n;sa	fp real	dp real	f.pt to blk exp
54	APLOGF	n;sa;sl;x;s	none	sp real	log freq axis
55	APBKPT	n;sa;sl;m;m;a;a	none	dp real	join dmnd bkpts
56	APISSU	ma	none	1200 words	o/p s/w issue

ARGUMENT CODES

be	block exponent
se	scale exponent
sm	scale mantissa
n	number of points
sa	start address in ap operand memory
ma	address in 1200 memory
ea	exponent address in 1200 memory
b	block count
la	1200 limit table address
d	dummy (set = 1)
t	type (0 = real, 1 = imag, 2 = cplx)
fh	factor ms word
fl	factor ls word
o	offset
sea	1200 address of exponent list
mea	1200 address of max exponent
da	destination address in ap operand memory
aa	address of average in ap operand memory
ke	average forgetting factor exponent
km	average forgetting factor mantissa
oe	offset exponent
om	offset mantissa
ts	source type (0 = real, 1 = imag, 2 = cplx)
td	destination type (0 = real, 1 = imag, 2 = cplx)
ar	angle range (0 = + or - pi, 1 = 0 to 2pi)
k	number of lines per resolution group
ca	address of comparison profiles in ap operand memory
sar	address of multiplier in ap operand memory
sac	address of multiplicand in ap operand memory
sap	address of product in ap operand memory
san	address of numerator in ap operand memory
sad	address of denominator in ap operand memory
saq	address of quotient in ap operand memory
r0	random number seed
sa1	address of time sequence 1 in ap operand memory
sa2	address of time sequence 2 in ap operand memory
dsa	address of delay store in ap operand memory
me	minimum exponent
ce	peak level exponent
cm	peak level mantissa
ra	address of reference demand level in ap operand memory
c	check profile level
l	1200 address of check result
m;m	dp minimum psd value
t;t	dp threshold to substitute for above
sl	starting ordinate number
x	x axis position of line #1
s	log scale factor = (lines span/log no of pts)*32log2
m;m	d.p. value of log slope (base 2) to next bkpt (P15 format)
a;a	exp; mant of psd at starting bkpt

8.3.3 ARRAY PROCSSOR REGISTERS

FFF8 (2FF0) Control (R/W)



Bit 0 (W) '1' = 'go', i.e. execute analysis task.

Bit 4 (R/W) '1' = interrupt on 'busy'.

Bit 6 (R/W) '1' = interrupt on 'ready'.

Bit 7 (R) '1' = array processor ready.

Bit 8 (W) '1' = abort present task.

Bit 9 (R) '1' = array processor busy.

FFF9 (2FF2) Input/Output Data (R/W)

input/output data word

FFFB (2FF6) FIFO Data (W)

FIFO data word

SECTION 8.4 GPIB INTERFACE

8.4.1 INTRODUCTION

The GPIB interface provides for remote control of the RVC from the general purpose interface bus (GPIB). The interface comprises three pcbs: board 5, which contains the GPIB control logic; board 6, which contains the GPIB-RVC Bus translation logic; and board 7, which is a small pcb containing the GPIB address switch. Plug PLC on board 5 connects to plug PLD on board 6, whilst plug PLD on board 5 connects to pcb 7.

8.4.2 TALK/LISTEN CONTROL

Talk/Listen control of the GPIB is exercised through an 8291 chip, IC6 on board 6. IC6 contains sixteen registers for communications via the RVC bus, eight for read only functions(data in and T/L status) and eight for write only functions (data out and T/L control). The bit functions of each of these registers are shown below, together with the register addresses.

		READ REGISTERS	REGISTER SELECT CODE RS2	RS1	RS0
FF20	(2E40)	DI7 | DI6 | DI5 | DI4 | DI3 | DI2 | DI1 | DI0 — DATA IN	0	0	0
FF21	(2E42)	CPT | APT | GET | END | DEC | ERR | BO | BI — INTERRUPT STATUS 1	0	0	1
FF22	(2E44)	INT | SPAS | LLO | REM | SPASC | LLOC | REMC | ADSC — INTERRUPT STATUS 2	0	1	0
FF23	(2E46)	S8 | SRQS | S6 | S5 | S4 | S3 | S2 | S1 — SERIAL POLL STATUS	0	1	1
FF24	(2E48)	ton | lon | EOI | LPAS | TPAS | LA | TA | MJMN — ADDRESS STATUS	1	0	0
FF25	(2E4A)	CPT7 | CPT6 | CPT5 | CPT4 | CPT3 | CPT2 | CPT1 | CPT0 — COMMAND PASS THROUGH	1	0	1
FF26	(2E4C)	X | DT0 | DL0 | AD5-0 | AD4-0 | AD3-0 | AD2-0 | AD1-0 — ADDRESS 0	1	1	0
FF27	(2E4E)	X | DT1 | DL1 | AD5-1 | AD4-1 | AD3-1 | AD2-1 | AD1-1 — ADDRESS 1	1	1	1

WRITE REGISTERS

									REGISTER SELECT CODE		
									RS2	RS1	RS0
FF00	(2E00)	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0	0	0	0
		DATA OUT										
FF01	(2E02)	CPT	APT	GET	END	DEC	ERR	BO	BI	0	0	1
		INTERRUPT ENABLE 1										
FF02	(2E04)	0	0	DMAO	DMAI	SPASC	LLOC	REMC	ADSC	0	1	0
		INTERRUPT ENABLE 2										
FF03	(2E06)	S8	rsv	S6	S5	S4	S3	S2	S1	0	1	1
		SERIAL POLL MODE										
FF04	(2E08)	TO	LO	0	0	0	0	ADM1	ADM0	1	0	0
		ADDRESS MODE										
FF05	(2E0A)	CNT2	CNT1	CNT0	COM4	COM3	COM2	COM1	COM0	1	0	1
		AUX MODE										
FF06	(2E0C)	ARS	DT	DL	AD5	AD4	AD3	AD2	AD1	1	1	0
		ADDRESS 0/1										
FF07	(2E0E)	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	1	1	1
		EOS										

8.4.3 DMA ADDRESS CONTROL

DMA addressing is controlled by a pair of AM2940 chips, IC7 and IC8 on board 5. These two chips are operated in cascade to generate a sixteen bit address, so the data loaded into the control register pairs must be identical, e.g. 0101. IC 7 and IC8 contain eight RVC bus registers, and the functions and addresses of these are shown below. The counters are initiated by writing to address FF0C.

TABLE I. Am2940 INSTRUCTIONS

	I_2 I_1 I_0	Octal Code	Function	Mnemonic	Control Mode	Word Reg.	Word Counter	Address Reg.	Address Counter	Control Register	Data D_0-D_7
FF08 (2E10)	L L L	0	WRITE CONTROL REGISTER	WRCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	D_0-D_2→CR	INPUT
FF09 (2E12)	L L H	1	READ CONTROL REGISTER	RDCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	CR→D_0-D_2 (Note 1)
FF0A (2E14)	L H L	2	READ WORD COUNTER	RDWC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	WC→D
FF0B (2E16)	L H H	3	READ ADDRESS COUNTER	RDAC	0 1 2 3	HOLD	HOLD	HOLD	HOLD	HOLD	AC→D
FF0C (2E18)	H L L	4	REINITIALIZE COUNTERS	REIN	0 2 3	HOLD	WCR→WC	HOLD	AR→AC	HOLD	Z
					1	HOLD	ZERO→WC	HOLD	AR→AC	HOLD	Z
FF0D (2E1A)	H L H	5	LOAD ADDRESS	LDAD	0 1 2 3	HOLD	HOLD	D→AR	D→AC	HOLD	INPUT
FF0E (2E1C)	H H L	6	LOAD WORD COUNT	LDWC	0, 2 3	D→WR	D→WC	HOLD	HOLD	HOLD	INPUT
					1	D→WR	ZERO→WC	HOLD	HOLD	HOLD	INPUT
FF0F (2E1E)	H H H	7	ENABLE COUNTERS	ENCT	0, 1, 3	HOLD	ENABLE COUNT	HOLD	ENABLE COUNT	HOLD	Z
					2	HOLD	HOLD	HOLD	ENABLE COUNT	HOLD	Z

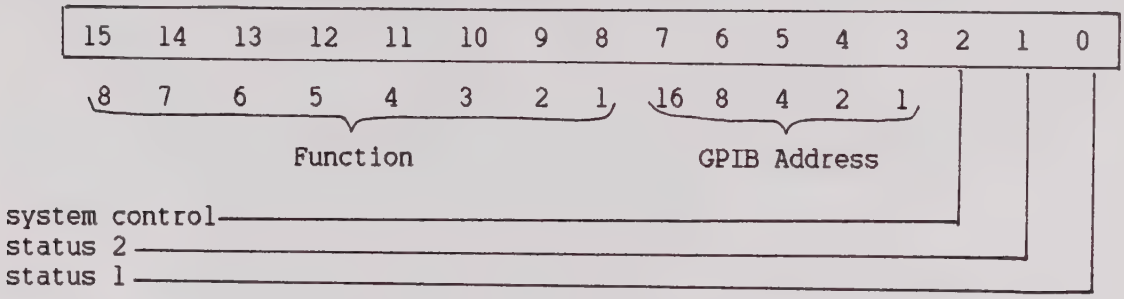
CR = Control Reg.
AR = Address Reg.
AC = Address Counter
WCR = Word Count Reg.
WC = Word Counter
D = Data
L = LOW
H = HIGH
Z = High Impedance

Note 1:
Data Bits D_3-D_7 are high during this instruction.

8.4.4 GPIB ADDRESS AND STATUS

The GPIB address and status of the RVC are read from register FF12, whose functions are shown below.

FF12 (2E24) GPIB Address/status Register (R)



Most of the data in register FF12 are set on the GPIB interface panel at the rear of the RVC. These data are:

GPIB function, bits 15-8
GPIB address, bits 7-3
system control, bit 2

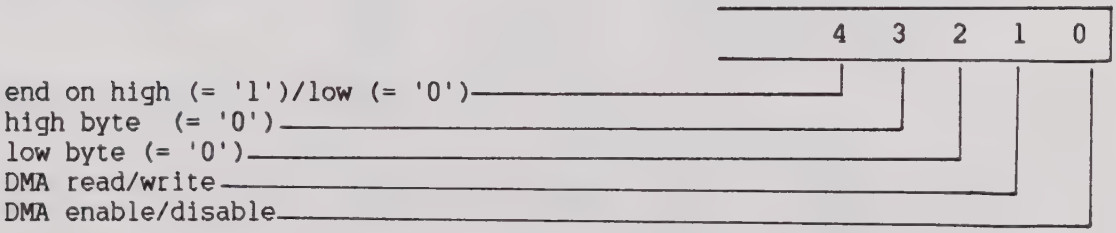
Bit 2 is set to '1' (SYSTEM CONTROL switch ON) when a GPIB controller chip is fitted to board 6.

Bits 1 and 0 are not set by the STATUS 1 and STATUS 2 switches. Bit 1 indicates the selection of a high or low data byte, for data transfers between the RVC bus and the GPIB; '1' = high byte, '0' = low byte. Bit 0 indicates the busy/finished state of a DMA data transfer' '1' = DMA transfer finished, '0' = DMA transfer in progress.

8.4.5 DMA CONTROL

DMA control of the GPIB interface is exercised through register FF13, whose functions are shown below.

FF13 (2E26) DMA CONTROL REGISTER (R/W)



Bit 0	Master control to enable or disable DMA; '1' = enable DMA, '0' = disable DMA.
Bit 1	'1' = DMA read cycle, '0' = DMA write cycle.
Bits 2, 3 & 4	work in combination to select the various ways in which 8 bit data are transferred to and from the 16 bit RVC bus.

The following table gives the options:

	End on H/L	High Byte	Low Byte	Options	
1	X	1	0	Low byte only	= Toggle
2	X	0	1	High byte only	X = Don't care
3	0	1		From high to low	
4	0		1	From low to low	
5	1	1		From high to high	
6	1		1	From low to high	

N.B. To start on the low byte, Toggle HIGH BYTE;
to start on the high byte, Toggle LOW BYTE.

The first three listed in the table are the only options currently used in the system.

Depending on the option used, the number of bytes transferred vary with the word count loaded in the 2940. In the following examples 4 was loaded into the word count register.

		H	L
(1)	For low byte only		✓
	(3 bytes)		✓
			✓
(2)	For high byte only	✓	
	(3 bytes)	✓	
		✓	
(3)	From high to low	✓	✓
	(6 bytes)	✓	✓
		✓	✓
(4)	From low to low		✓
	(5 bytes)	✓	✓
		✓	✓
(5)	From high to high	✓	✓
	(7 bytes)	✓	✓
		✓	✓
		✓	
(6)	From low to high		✓
	(6 bytes)	✓	✓
		✓	✓
			✓

8.4.4 INTERRUPTS

Interrupt level 7: GPIB T/L or DMA done.
Interrupt level 8: GPIB controller.

Bit 0 of the GPIB Address/Status register (FF12) is looked at to determine which of the two interrupted at level 7.

Bit 0 is set if it was DMA done that interrupted.

When the GPIB controller is not plugged into Board 6 a header with the following connections is inserted in place of it.

(1) IC7 pin 24	tied to GND
(2) IC7 pin 29	tied to VCC
(3) IC7 pin 31	tied to VCC
(4) IC7 pin 32,33,35	tied to GND
(5) IC7 pin 36	tied to VCC

8.4.7 DMA SETUP SEQUENCE

For a DMA transfer, the following setup sequence is suggested:

	Address	Data	
GPIB Controller	FF10	84	Mask out all interrupts.
GPIB T/L	FF25	2	Reset chip.
	FF24	1	Select addressing mode 1.
	FF21	0	Mask out all interrupts
	FF22	0	Mask out all interrupts
	FF26	0	Load major address.
	FF26	E0	Load minor address.
	FF25	26	Preset internal counter.
	FF25	0	Release initialisation status.
Address Generator	FF08	---(eg 101)	Load control register.
	FF0D	---(eg 0)	Load status address.
	FF0E	---(eg 10)	Load word count.
DMA mode register	FF13	---(eg 1B for DMA out 19 for DMA in)	
GPIB T/L	FF22	20 (Start DMA out) 10 (Start DMA in)	Enable appropriate. DMAO, DMAI mask.

The same DMA cycle can be repeated, with the same start address and word count, by writing to the address generator at address FF0C.

SECTION 8.5 DATA STORE

8.5.1 INTRODUCTION

The data store is situated on board 4 and consists of a memory array accessed as a slave by other modules on the RVC bus.

8.5.2 RAM ARRAY

The main RAM array has a capacity of 48K words and comprises forty eight MK4116 16K x 1 dynamic RAM memories. These are refreshed by a controller type 8202A (IC51). The controller receives READ and WRITE requests from the RVC bus and on completion of a refresh cycle performs the required memory operation and generates the ACK signal. When the READ or WRITE is removed, the controller resumes its refresh activity.

8.5.3 NON-VOLATILE STORE

Also contained on board 4 are four HM6514 CMOS RAMS and a Ni-Cd battery to power them during power interruptions. In normal use the battery is charged via TR3 andd R25, but when the power is removed TR3 turns off and the battery takes over the supply of the RAMs via D3.

To protect the data during power down, TR1 detects a drop in Vcc below 4.7 volts (before the battery takes over at 3 volts) and turns off TR2. This causes all the CMOS RAMs to be disabled and thus maintains the data integrity.

When power is restored, the reverse sequence occurs. TR3 turns on, providing power to the RAMs and charging the battery, then TR1 turns on and enables the RAMs to be accessed.

The non-volatile store is addressed on the RVC bus at addresses E000-E3FF (1K words).

SECTION 8.6 DISPLAY INTERFACE

8.6.1 INTRODUCTION

The display interface translates the analysis data and the associated annotation data into a form suitable for display. In addition to driving the RVC CRT the interface provides an output suitable for a video monitor or a video printer.

8.6.2 DISPLAY DATA FLOW

The analysis data are received from the array processor, whilst the annotation data are received from the system controller. In each case, the data are written into the data buffer in the display interface internal memory, under the DMA control of the source module. Data translation is done by a 16 bit microprocessor (type TMS 9900). This acts in accordance with a command string that is written by the system controller into the command buffer which, again, is in the display interface memory. Commands for graphics data are given priority 'A', whilst commands for annotation data are given priority 'B'. The latter commands have the top priority; a graphics translation may be interrupted for an annotation translation but not vice versa. Priority is imparted by writing the commands into a specfic command buffer area, defined as follows: addresses EC00 to EC3F for low priority (A) commands and addresses EC40 to EC7F for high priority (B) commands. The data buffer is defined by addresses E800 to EBFF. A list of translation commands and associated parameters is given in Table 8.7.

A block diagram of the display interface hardware appears in Fig. 8.9. This shows the basic signal flow through board 3 (display buffer and control) and board 2 (video store and drive).

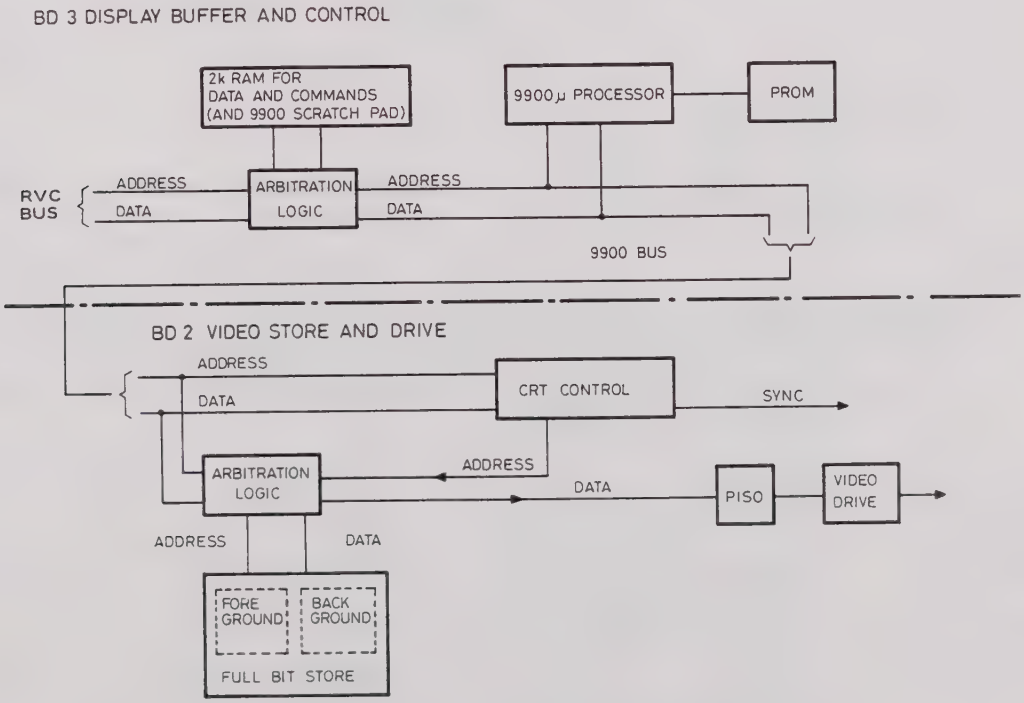


Fig. 8.9 Display interface signal flow

8.6.3 DISPLAY DATA PROCESSING

On board 3 the microprocessor (IC 24) translates the contents of the data buffer, in accordance with the command string. The command codes and parameters are decoded by the program contained in a 4k PROM (ICs 11, 12, 42 and 43). The results of translation, in the form of a display bit pattern, are routed by the microprocessor to the 'full bit' store on board 2.

The full bit store is so named for the simple reason that it can hold enough bits of data for a full screen of information. It can, in fact, hold enough bits to fill the screen twice and is used in a 'foreground/background' mode. While one half of the store is being updated by the microprocessor the other half is producing data for display; when updating is complete these roles are reversed and updating begins on the other half of the store.

Board 2 also contains the CRT control chip (IC 31). This organises the display of data from the full bit store, in synchronism with the raster scan. Each data word accessed by IC 31 is converted into serial-by-bit form by two 'parallel in, serial out' chips (ICs 7 and 20) and is suitably ampilfied before application to the video amplifier of the CRT assembly.

'Start', 'interrupt enable' and 'abort' control of a display data translation sequence is achieved through register FF40 (display control).

Table 8.7 Display Command Codes

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COMANDS AND PARAMETER LIST.

Data buffer - E800 › EBFF

Low priority command buffer - EC00 › EC3F
High priority " " - EC40 › EC7F

NOTES:

Vertical position is by scan line number; line 0 is top & EF bottom.
Horizontal position is by column number; 0 is at left & 21F at right.
Graph data points are relative to the defined lower graph limit; 0 at the bottom.
Graph and cursor x-axis data are relative to the graphical area, which starts at column #20.

COMMAND	CODE	FUNCTION	PARAMETERS	COMMENTS
DPBOOT	00	initialise display	none	
DPINBP	01	load crt chip for 60 hz.	none	
DPEXEC	02	exec. temp prog.	none	
DPNOOP	03	no-op	none	
DPREPT	04	repeat commands	none	
DPCLRC	05	clear current write half	none	
DPCLRD	08	clear defined area	first last	address in fbs 8000 › BFFF

Table 8.7 Cont

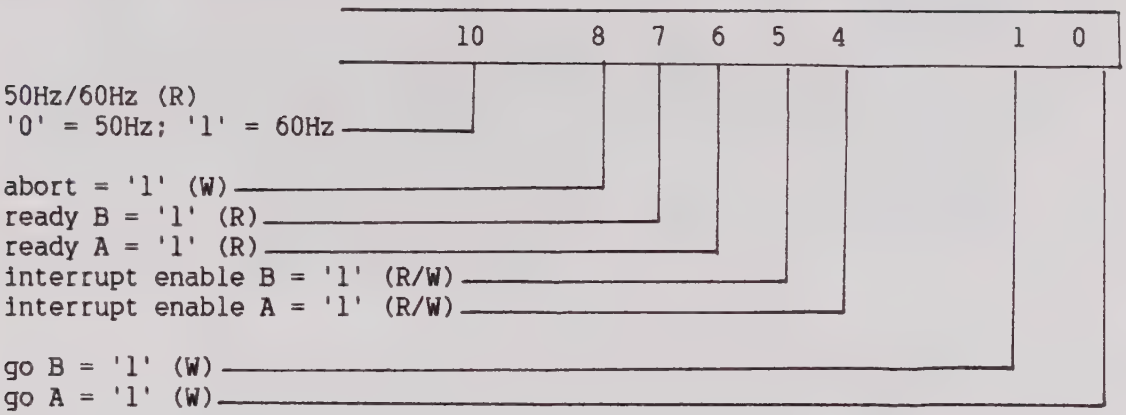
DPTXT	09	write text from data buffer first byte address relative to E800		
		control bytes in text :-		
		#00	end of text string.	
		#0B	next byte is row number (0) #1D).	
		#0C	screen erase.	
		#0D	c/r & l/f.	
		#0E	clear reverse video.	
		#0F	set reverse video.	
		#10	next byte is col. number (0) #43).	
		#19	decimal point (no width).	
DPVERT	0B	plot with vert join	number of pts	
			first	byte addr rel to E800
			first x	col rel to graph area
			top limit	0) EF, 0 = top
			bottom limit	0) EF, EF = bottom
			x expansion	1) #10 times
DPVECT	0C	plot with vector join	number of pts	
			first x data	byte addr rel to E800
			first y data	byte addr rel to E800
			top limit	0) EF, 0 = top
			bottom limit	0) EF, EF = bottom
			x expansion	not used
DPAA	0E	write A / display A	none	
DPAB	0F	write A / display B	none	
DPBA	10	write B / display A	none	
DPBB	11	write B / display B	none	
DPSWAP	12	swap write & display	none	
DPCUON	14	enable cursors	none	
DPCUOF	15	disable cursors	none	
DPDRWH	16	draw horizontal line	scan line	0) EF
			left col	0) 21F
			right col	0) 21F
DPDRWV	17	draw vertical line	column	0) 21F
			top scan line	0) EF
			bottom scan	0) EF
DPDRWB	18	draw line box	top scan	0) EF
			bottom scan	0) EF
			left column	0) 21F
			right column	0) 21F
DPCLRH	19	clear horizontal line	scan line	0) EF
			left col	0) 21F
			right col	0) 21F
DPCLRV	1A	clear vertical line	column	0) 21F
			top scan line	0) EF
			bottom scan	0) EF
DPCLRB	1B	clear solid area	top scan	0) EF
			bottom scan	0) EF
			left column	0) 21F
			right column	0) 21F
DPCLRR	1C	clear open box	top scan	0) EF
			bottom scan	0) EF
			left column	0) 21F
			right column	0) 21F

Table 8.7 Cont

DPWRTS	1D	write to seen half	none	
DPWRTD	1E	write to unseen half	none	
DPDCA	1F	define vertical cursor	top scan	Ø) EF
			bottom scan	Ø) EF
DPDCH	22	define horiz cursor	left column	Ø) 1FF
			right column	Ø) 1FF
DPLCA	23	load vertical cursor	column	Ø) 1FF
DPLCH	26	load horiz cursor	scan	Ø) EF
DPCCA	27	clear vert cursor	column	Ø) 1FF
DPCCH	2A	clear horiz cursor	scan	Ø) EF
DPCACA	2B	clear vert definition	none	
DPCACH	2E	clear horiz definition	none	
DPCAC	30	clear all cursors	none	
DPVGRT	31	draw vert. graticule	column	Ø) 1FF
DPHGRT	32	draw horiz. graticule	scan	Ø) EF
DPGROF	33	erase graticule	none	
DPREVV	34	set reverse video	none	
DPNRMV	35	clear reverse video	none	
DPXHCH	36	crosshatch pattern	spacing	
DPLIMT	37	set cursor limits	top scan	Ø) EF
			bottom scan	Ø) EF
			left column	Ø) 1FF
			right column	Ø) 1FF
DPTEST	38	self-test & s/w issue	none	

8.6.4 DISPLAY REGISTER

FF40 (2E80) Display Control (R/W)



Notes: 1. To clear bits 6 and 7 (ready), set bits 1 and 2 (go) and bit 8 (abort) to '1'.

2. Bits 4 and 5 (interrupt enable) may be set at the same time as bits 1 and 2 (go) or bit 8 (abort) without causing spurious interrupts.

3. On completion of an abort (boot) operation, bits 6 and 7 (ready) are both set to '1'. All other bits are set to '0'.

SECTION 8.7 PLOTTER INTERFACE

8.7.1 INTRODUCTION

The X, Y plotter receives X and Y co-ordinate data directly from the controller. This data is derived from the display co-ordinate data and provides for a hard copy of the displayed analysis functon, with optional axis annotation. The X and Y data are written into separate registers.

8.7.2 PLOTTER CONTROL

Plotter control is achieved via a single register containing only two bits. One bit is for pen up/down control, whilst the other is for accessing the timer that is used to define the plotter speed.

8.7.3 SERIAL LINK BAUD RATE

For convenience, the switch that is used to select the Baud rate for data transfers on the 'serial link' (RS 423) is mounted on the rear panel of the plotter module. The switch setting is read through the Baud rate register of the plotter module.

8.7.4 PLOTTER REGISTERS

FF14 (2E28) RS 423 Baud Rate (R)

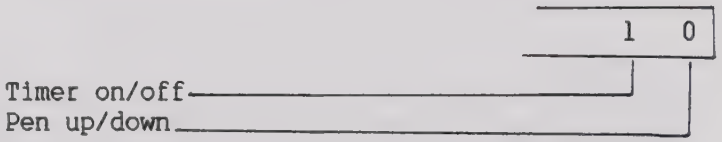
7	6	5	4	3	2	1	0
Baud rate				1s complement of Baud rate			

Baud rate switch settings;

0	0	0	0	0	1	1	1	1
(1)	0	0	0	1	1	1	1	0
2	0	0	1	0	1	1	0	1
(3)	0	0	1	1	1	1	0	0
		etc.			etc.			

The switch settings in brackets are unmarked.

FF15 (2E2A) Plotter Control (W)



Bit 0 Pen Up/down Control

The pen control contact closures, accessible via a 15 way Cannon socket on the rear of the plotter module, operate as follows:

Socket pins 13, 14	Socket pins 14, 15	Control State
contact closed	contact open	1(= pen up)
contact open	contact closed	0(= pen down)

Bit 1 Timer On/off Control
The timer is used by the system controller as a time reference in determining the rate at which data are written into the plotter data registers.

1ms after bit 1 is set, the plotter module requests an interrupt. By repeatedly setting (and resetting) bit 1 and counting the resultant interrupt requests the controller is able to define the X, Y data periods, to a resolution of 1ms. The count made is in accordance with the plotting speed selected by the user (via the plotter FORMAT menu).

FF16 (2E2C) X Channel Data (W) and
FF17 (2E2E) Y Channel Data (W)

9	8	7	6	5	4	3	2	1	0

X or Y co-ordinate

The X and Y co-ordinate data are each presented by a 10 bit number between 0 and 1023 (decimal). Each number is converted into an analogue voltage to drive a plotter. The maximum value, 1023, corresponds to an analogue output of 10V, adjustable by RV1 for the X channel and RV2 for the Y channel. This gives a drive resolution of approximately 10mV. The X and Y analogue outputs can be monitored on the 15 way Cannon socket at the rear of the plotter module. The connections are as follows:

Socket pin	Function
1	ground (0v)
2	X channel output
3	Y channel output
4	ground

SECTION 8.8 KEYBOARD INTERFACE

8.8.1 INTRODUCTION

The keyboard interface translates the commands keyed into the RVC into an eight bit command word for the system controller. The command word is sent to the controller via a serial link.

The commands are divided into two groups: those from the key panel, which give a key code, and those from the keyswitch and interlock remote sensing input, which give a status word. Status words have the highest priority; if a change in status occurs while key codes are being sent to the controller the interface switches to sending the new status word. On acknowledgement of the new status from the system controller, the keyboard interface is again able to send key codes.

Two functions of the keyboard interface can be controlled from the system controller. These are the bleeper, and the 'interlock ready' contacts. Also, to show that it has acknowledged a change in status, the controller must send the new status code back to the keyboard interface. An eight bit data word which controls these functions is received from the system controller via the serial link.

8.8.2 OUTPUT DATA WORD

The significance of a data word output by the keyboard is defined by bit 6; a '1' state (Hi) indicates a status word, whilst a '0' state indicates a key code.

Bits 0 to 3 of the status word are merely the four least significant bits of the last key code input, and are ignored by the controller. The functions of the remaining bits are as follows:

Bits 4 and 5: Keyswitch Code

Bit 4	Bit 5	Function
0	0	Remote
1	0	Local
0	1	Program

Bit 7: Interlock Status

0 = 'ready' contacts open; '1' = 'ready' contacts closed.

Each key code (signified by a '0' in bit 6) consists of two hexadecimal digits. A full list of codes, with the corresponding key functions, appears in Table 8.8.

8.8.3 INPUT DATA WORD

The input data word contains:

a) the commands that allow the system controller to control the bleeper and the 'interlock ready' contacts, and
b) the status data with which the controller acknowledges a status change.

The bit functions of the input data word are:

Bit 0: 'Interlock Ready' Contacts

'0' = open 'ready' contacts; '1' = close 'ready' contacts.

Bit 1: Short Bleep Enable

'0' = disable short bleep; '1' = enable short bleep.

Bit 2: Long Bleep Enable

'0' = bleeper off; '1' = bleeper on.

The '1' state of bit 2 also enables the function of bit 0, after a reset has occurred.

Bit 3; Status Word Request

'0' = allow key code transfers; '1' = send status word to controller.

8.8.4 CIRCUIT OPERATION

A block diagram of the keyboard interface, showing the main data paths is given in Fig 8.10. The circuit diagram (12107553) appears in Chapter 10.

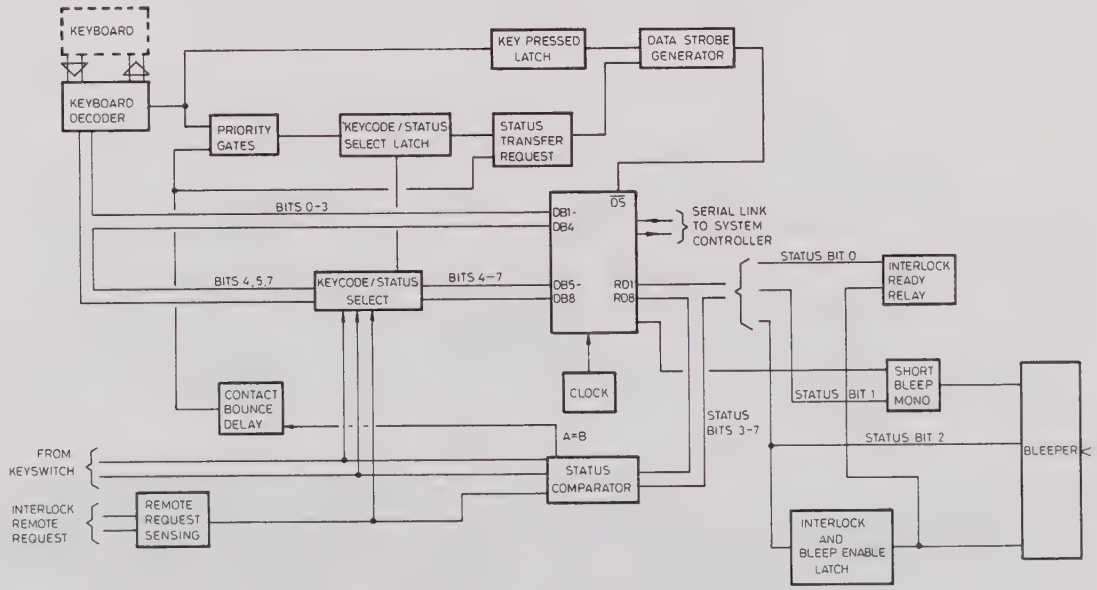


Fig 8.10 Keyboard Interface

8.8.4.1 Data Transfers

Data transfers between the keyboard interface and the system controller are managed by a UART (universal asynchronous receiver/ transmitter). This can receive key codes from the **Keyboard Decoder** or status words from **Remote Request Sensing** and the front panel keyswitch. For each word, from either source, the **Data Strobe Generator** produces a $\overline{DS}$ (data strobe) pulse when the data is valid, and this is applied to the UART to start the data transfer. For a key code the Data Strobe Generator is triggered from the **Key Pressed Latch**, whilst for a status word it is triggered from the **Status Transfer Request Gate**. The data strobe timing is shown in Fig 8.11.

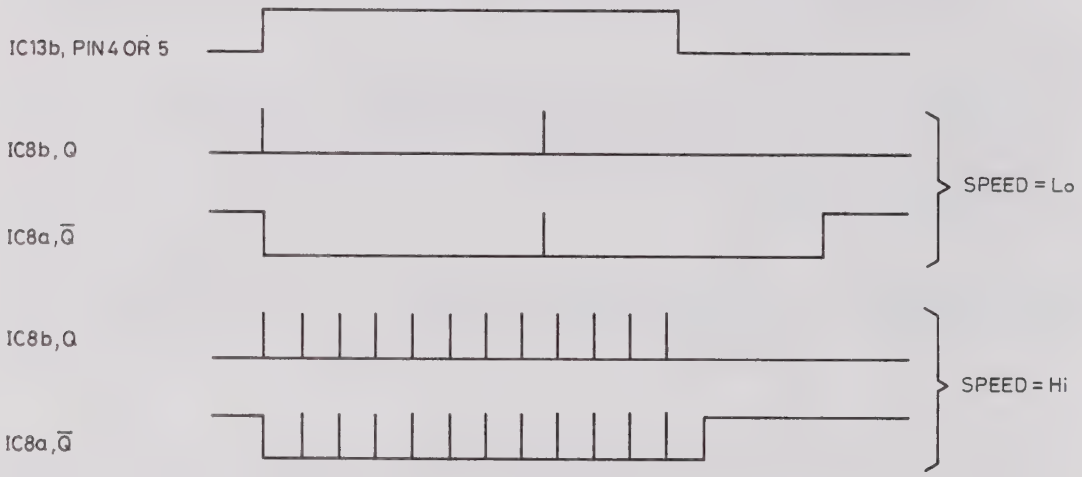


Fig 8.11 Data strobe generator timing

8.8.4.2 Key Code/ Status Selection

The selection of a key code or a status word is achieved by **Key Code/ Status Select**. A key code uses bits 0 to 7, whilst a status word uses bits 4 to 7 only; therefore word selection is made on bits 4 to 7 and the system controller is programmed to ignore bits 0 to 3 of a status word. Bit 6 of a key code or status word is inserted by Key Code/ Status Select: '0' = key code and '1' = status word. Key Code/ Status Select is controlled from the **Key Code/ Status Select Latch**, which is set from the Priority Gates.

8.8.4.3 Priority Gates

Key presses and status changes occur asynchronously and the purpose of the **Priority Gates** is to arbitrate between the two, whilst giving status changes the top priority. A circuit detail of the Priority Gates is given in Fig 8.12. On system initialisation the RESET signal sets the Key code/ Status Select Latch, IC3a, to the 'status' state (Q = Hi; $\overline{Q}$ = Lo) and thereafter the priority gates act to keep this as the preferred state. While the RVC status remains unchanged, a key press sets IC3a to the key code state (Q = Lo; $\overline{Q}$ = Hi), but on completion IC3a is clocked

back to the status state via IC14a. At any time during a key press, except when a key code transfer is actually taking place, the priority gates can act on a Hi status change signal to clock IC3a to the status state, thus changing an intended key code transfer into a status transfer. The timing diagram for this is shown in Fig 8.13. If the key of an interrupted key code transfer is still pressed after the status change has been acknowledged then IC3a will be set back to the key code select state until transference of the key code(s) is completed.

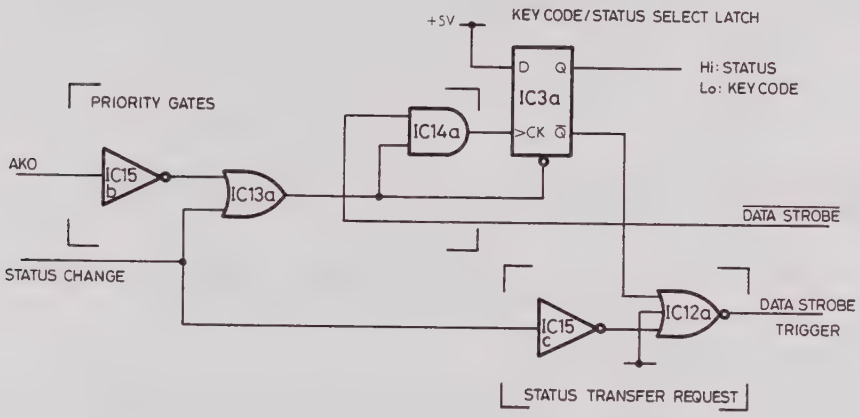


Fig. 8.12 Priority Gates

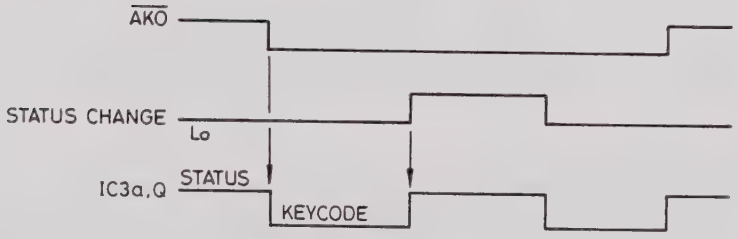


Fig. 8.13 Status Change Timing

8.8.4.4 Keyboard Decoding

For each key press on the keyboard matrix the **Keyboard Decoder** (IC1) produces a two digit hexadecimal code (see Table 8.8), which is applied to the data buffer inputs of the UART. An 'any key down' output (AKO) from the decoder is taken Hi for the duration of the key press and this signal is applied to the Priority Gates where, if a status change is not being attended to, it causes the Key Code/ Status Select Latch to be set to the key code state (see Fig. 8.14). When the key code of the present key press is ready, the DATA READY output of the decoder is pulsed Hi and this clears the **Key Pressed Latch** (IC3b) to the 'key pressed' state (Q = LO; $\bar{Q}$ = Hi). The Lo Q output lights the 'key pressed' lamp (LED1),

whilst the Hi $\overline{Q}$ output triggers the Data Strobe Generator. When a key is released the AKO output, in going Lo, presets the Key Pressed Latch to the 'key not pressed' state; the Hi Q output switches off the 'key pressed' LED, whilst the Lo Q output stops the Data Strobe Generator from producing a further $\overline{DS}$ pulse.

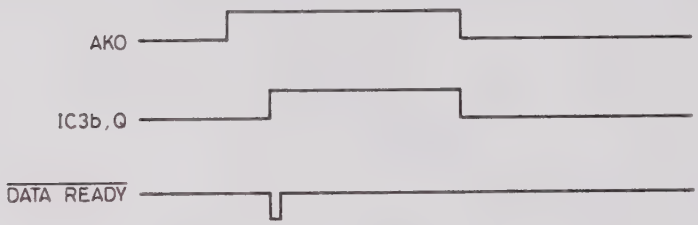


Fig. 8.14 Keyboard Decoder Timing

8.8.4.5 Status Change Detect
A status change is detected by the Status Comparator (IC6) This chip compares the state of the keyswitch and the interlock input with the state of corresponding status bits held in the UART read data register. Any difference between the two causes the A = B output of IC6 to go Lo, which in turn causes the Status Change Latch to be set, via the Contact Bounce Delay, to the 'status changed' state (IC4a, Q = Hi).

The Hi 'status changed' signal is applied,

a) to the Priority Gates, where it ensures that the status word is applied to the UART data buffer inputs, and
b) to the Status Transfer Request Gate, from which, if condition a) is satisfied, it triggers the Data Strobe Generator.

8.8.4.6 Status Acknowledge
When the system controller receives a status word from the keyboard interface, it sets up the RVC according to the data contained in bits 4 to 7 and sends the same data back to be stored in the UART read data register. The Status Comparator now detects the equality state and its Hi A = B output resets the Status Change Latch, thus releasing the keyboard interface for use with the key codes.

8.8.4.7 Interlock Ready and Bleeper Control
Bits 0 to 3 of the status word sent by the system controller are used to control the 'interlock ready' relay and the bleeper, as follows:

Bit 0: 'Interlock Ready' Control

'1' (= Hi) energises relay: contacts closed;
'0' (= Lo) de-energises relay: contacts open.

Bit 1: Short Bleep Control

'1' (= Hi) enables Short Bleep Monostable. Monostable triggered each time the DAV (data available) output of the UART goes Hi.

'0' (= Lo) disables Short Bleep Monostable.

Bit 2: Long Bleep Control

'1' (= Hi) switches bleeper on (and enables the bleeper and the 'interlock ready' relay after initialisation).

'0' (= Lo) switches bleeper off.

Bit 3: Interrogate Status

'1' (= Hi) holds the 'status change' input of the Priority Gates Hi to allow the system controller to read the keyboard status.

'0' (=Lo) releases keyboard interface for key code use.

Table 8.8 Key Codes

Code	Function	Code	Function
00	-	23	-
01	-	24	-
02		25	-
03		26	Level Sequence
04	Soft Key 6	27	Status
05	Soft Key 5	28	6
06	Soft Key 4	29	5
07	Soft Key 3	2A	4
08	Soft Key 2	2B	Back Space
09	Soft Key 1	2C	-
0A	-	2D	-
0B	-	2E	Run Low
0C	-	2F	Set Input
0D	-	30	Demand psd
0E	-	31	Overlay
0F	-	32	9
10	Analyse	33	8
11	Drive Limits	34	7
12	Plot	35	+/-
13	Freeze	36	horizontal cursor
14	Enter	37	vertical cursor
15	.	38	Run High
16	0	39	Set Analysis
17	E Ex	3A	Test Number
18	Abort	3B	Main
19	-	3C	Return to Local (rtl)
1A	Calibrate	3D	Self Test
1B	Drive	3E	-
1C	Protect Limits	3F	-
1D	Scale		
1E	2		
1F	3		
20	1		
21	Clear		
22	Hold		

CHAPTER 9

CRT REPLACEMENT

CONTENTS

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9.1 INTRODUCTION

This chapter contains full instructions for the removal of a faulty CRT tube from the RVC and for the installation of a new one. Before any of this work is attempted, however, particular attention should be paid to the CRT hazard warning.

9.2 CRT HAZARD WARNING

Users of cathode ray tubes should be aware of the hazards associated with these devices, which are:

a) implosion
b) X-rays
c) high voltage

These can occur in one or more of the following situations:

a) Storage and transport
b) Handling during replacement or installation
c) Operation
d) Disposal at the end of life.

9.2.1 Storage and Transport

The likelihood of implosion is minimised by storage in the approved transport packs at a reasonable temperature. The tube should be transported in the pack in which it is received from the supplier.

9.2.2 Handling and Fitting

An exposed cathode ray tube is potentially dangerous and extreme care must be taken to avoid causing an implosion.

The following precautions should be taken when handling the tube:

a) In the course of unpacking, installation or replacement, avoid scratching or damaging the tube in any way. Any such damage can reduce the strength of the glass envelope and result in an implosion, either instantaneously or subsequently.

b) Protective goggles and clothing should be worn.

c) No stresses should be imposed on the glass envelope, particularly at the neck. The tube should be handled by holding the cone and faceplate only.

d) Avoid subjecting the cathode ray tube to mechanical or thermal shock, e.g. knocking the tube off the bench, or touching it with a hot soldering iron. Any such shock can cause an implosion.

e) To minimise the risk of scratches, a free standing tube should be placed face down on a soft surface, such as rubber or cloth, which is free of abrasive particles. Otherwise, the tube should be placed in a support designed for it.

f) Particular attention is called to the fact that a high voltage charge can be carried by the internal conductive coating that is connected to the final anode connector of the tube, and also by the external coating if not earthed. The charge may remain even after the tube has been removed from the equipment. Anyone handling such a tube could receive an electric shock which, although not dangerous in itself, might cause an involuntary reaction and result in the tube being dropped.

It is recommended, therefore, that a tube is discharged before being handled. This applies to any tube in any situation. Discharge is best accomplished by earthing the EHT connector and external coating for one minute.

9.2.3 Operation

Dangers occur due to the possibility of electrical shock from the high potentials that are applied to the tube.

When a CRT is supplied with an external metal collar or metal shield, this should be connected to an adequate earth.

X-rays may be radiated when operating at voltages in excess of 16kV (in the RVC the EHT voltage is normally about 12.5kV). X-rays become progressively more harmful as the EHT voltage is increased. The glass envelope is an effective X-ray shield at lower voltages, but in cases where high voltages are used additional precautions should be taken.

To obtain full information on X-ray radiation hazards and precautions, reference should be made to Ionising Radiations (Sealed Sources) Regulations 1969 and to the Tube Data Sheet.

9.2.4 Disposal

Care should be taken by the user to ensure the safe disposal of the tube at the end of its useful working life.

The tube should be rendered harmless by placing it in a steel container face down and breaking the neck with a hard object. Protective goggles and clothing should be worn during this operation.

Alternatively, the tube can be returned to the original supplier, in the approved transport pack, with written authorisation for disposal.

9.3 CRT REMOVAL

1. Remove RVC from ac supply.

2. Remove RVC top and bottom covers.

3. Release the RVC front panel and tilt it forward into the servicing position.

4. Disconnect:

   Cables from PLA and PLB on RVC motherboard,
   POWER SWITCH connection.

5. Remove the screws securing the front panel hinge plates to the main chassis, lift the panel out and place it face downwards on the bench.

6. Remove EHT supply cable from CRT anode terminal.

7. Earth the anode terminal and external coating to dissipate any accumulated charge.

8. Ease off the remaining pan head screw securing the Digivision chassis and remove the connections from plugs PLB, PLC and PLD on the horizontal time base module (see Fig. 9.1.).

9. Remove the Digivision chassis securing screws completely and place the chassis to one side.

10. Remove the Digivision chassis mounting pillars and M6 nuts securing the CRT. Note the orientation of the CRT and then lift the CRT clear. The disposal instructions for the CRT are given on page 9.2.

9.4 CRT INSTALLATION

1. If the CRT removed was of the old type, with an additional glass plate at the front, then the new type of CRT mounting pillars (part no. 12002045A) should be fitted.

2. On the CRT mounting pillars, screw halfnuts to bottom of thread.

3. Wearing a protective apron and goggles, remove CRT from transit chassis and position on pillars. Adjust halfnuts to just touch CRT mounting brackets.

4. Fit Dag lead as shown in Fig. 9.2 and secure CRT using two M6 plain washers, two M6 crinkle washers, two M6 halfnuts and the Digivision chassis mounting pillars.

5. Plug black flylead from Dag lead onto video amplifier on CRT base; the wire may fit on either pin.

6. Remove the three Digivision pcb's from transit chassis and, using board supports (part no. 412011170), fit to Digivision chassis.

7. Fit Division chassis to mounting pillars using two M6 x 10 panhead screws and two M6 crinkle washers. Fit ring tag of earth lead in cableform under the lower screw, with the tag facing inwards.

8. Reconnect cables to plugs PLB, PLC and PLD on horizontal timebase module.

9. Refit front panel to RVC main frame.

10. Reconnect power switch.

11. Reconnect cables to plugs PLA and PLB on RVC motherboard.

12. Move front panel back into operating position and refit RVC top and bottom covers.

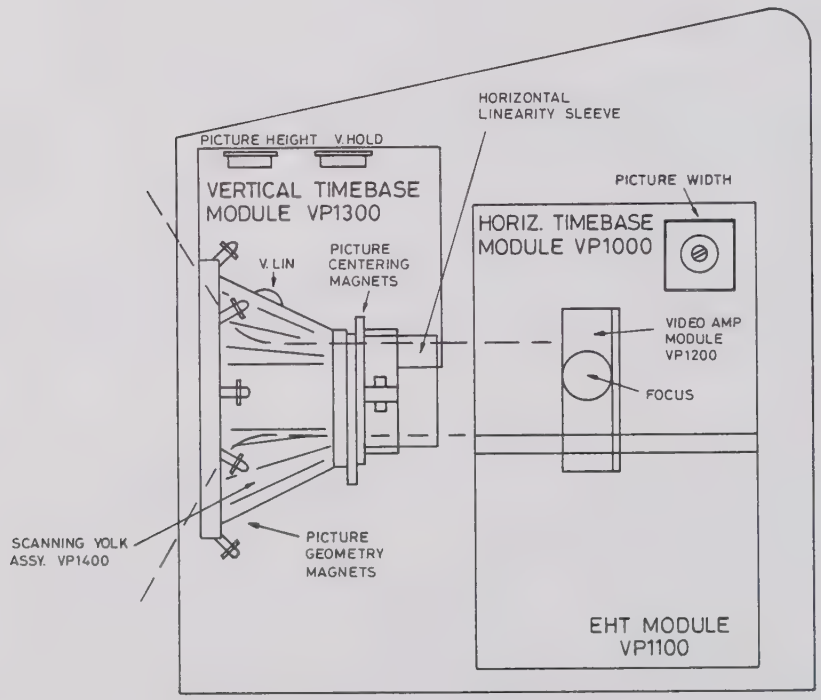

Fig. 9.1 RVC video assembly

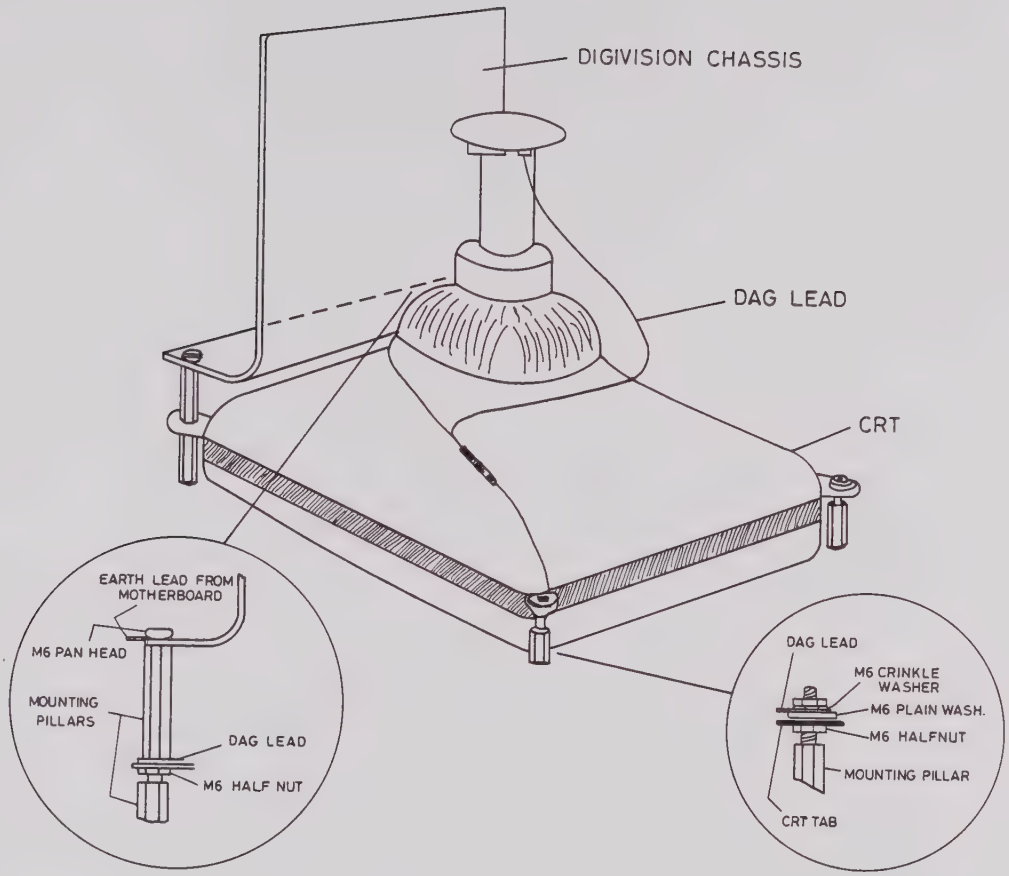

Fig. 9.2 CRT mounting

CHAPTER 10

Components Parts List

and

Circuit Diagrams

COMPONENT PARTS LIST ABBREVIATIONS

AE	Aerial	R	Resistor (Ω)
B	Battery	RE	Recording instrument
C	Capacitor (μF)	RL	Relay
CSR	Thyristor	S	Switch
D	Diode	SK	Socket
FS	Fuse	T	Transformer
IC	Integrated Circuit	TP	Terminal Post (or Test Point)
L	Inductor	TR	Transistor
LP	Lamp (including Neon)	V	Valve
LK	Link	X	Other Components
M	Motor		
ME	Meter	Also used:	
MSP	Mains Selector Panel	RNL	Non Linear Resistor (Ω)
PL	Plug	RV	Variable Resistor (Ω)

COMPONENT TYPES

Fixed Resistors

Carbon Composition	CACP
Carbon Film	CAFM
Cracked Carbon	CKCA
Metal Film	MEFM
Metal Oxide	MEOX
Power Wirewound	POWW
Precision Wirewound	PRWW
Temperature Sensitive	TEMP
Thick Film	TKFM
Thin Film	TNFM
Voltage Sensitive	VOLT

Variable Resistors

Carbon Front Panel Multiturn	CAFM
Carbon Front Panel Single Turn	CAFS
Carbon Preset Multiturn	CAPM
Carbon Preset Single Turn	CAPS
Cermet Front Panel Multiturn	CMFM
Cermet Front Panel Single Turn	CMFS
Cermet Preset Multiturn	CMPM
Cermet Preset Single Turn	CMPS
Wirewound Front Panel Multiturn	WWFM
Wirewound Front Panel Single Turn	WWFS
Wirewound Preset Multiturn	WWPM
Wirewound Preset Single Turn	WWPS

Capacitors

Air	AIR
Aluminium Electroyltic	ALME
Aluminium Solid	ALMS
Polycarbonate	CARB
Ceramic	CERM
Polyester Foil	ESTF
Polyester Metallised	ESTM
Glass	GLAS
Mica	MICA
Metalised Lacquer	MLAC
Paper Foil	PAPF
Paper Metallised	PAPM
PTFE	PTFE
Polypropylene Film	PYLN
Polystyrene	STYR
Tantalum Dry	TAND
Tantalum Foil	TANF
Tantalum Wet	TANW

PCB 1

Cct Ref.	General Description				Solartron Part No.
R1	MEOX	4.7k	¼W	1%	195334700
R2	MEOX	4.7k	¼W	1%	195334700
R3	MEOX	10k	¼W	1%	195341000
R4	MEOX	1k	¼W	1%	195331000
R5	MEOX	3.9k	¼W	1%	195333900
R6 to R9	MEOX	10	¼W	1%	195311000
R10	MEOX	1k	¼W	1%	195331000
R11	MEOX	2.2k	¼W	1%	195332200
R12	MEOX	330	¼W	1%	195323300
R13 to R16	MEOX	4.7k	¼W	1%	195334700
R17	MEOX	470	¼W	1%	195324700
R18	MEOX	2.2k	¼W	1%	195332200
R19	MEOX	330	¼W	1%	195323300
R20	MEOX	1k	¼W	1%	195331000
R21	MEOX	470	¼W	1%	195324700
R22	MEOX	1k	¼W	1%	195331000
R23 to R28	MEOX	4.7k	¼W	1%	195334700
R29	MEOX	6.8k	¼W	1%	195336800
R30	MEOX	1k	¼W	1%	195331000
R31	MEOX	1.5k	¼W	1%	195331500
R32	MEOX	1k	¼W	1%	195331000
R33 to R35	MEOX	4.7k	¼W	1%	195334700
C1 to C3	TAND	10	20V	20%	265871000
C4 to C22	CERM	.047		+50% -25%	241944700
C23	TAND	100	20V	20%	265881000
C24	ESTF	10p	125V	10%	210211000
C25	CERM	100p	500V	20%	241321000

PCB 1

Cct Ref.	General Description				Solartron Part No.
C26 to C29	CERM	47p	500V	20%	241314700
C30	TAND	10	20V	20%	265871000
C31 to C42	CERM	.047		+50% -25%	241944700
TR1	BCY70				300553590
TR2	BC107				300553320
IC1	SN74LS11N				510003110
IC2	SN74LS193N				510003580
IC3	SN74LS74N				510002600
IC4	SN74LS161AN				510004160
IC5	TMS9902JL				510004930
IC6*	F682 0106				12005203AA
IC6	2716				510003080
IC7	MK4118-3				510004730
IC8*	F642 0108				12005202AA
IC8	2716				510003080
IC9	MK4118-3				510004730
IC10	SN74LS10N				510002870
IC11	SN74LS374N				510004390
IC12	SN74LS30N				510003560
IC13	MC14020				510001830
IC14	TMS9900JL				510004920
IC15	SN74S74				510002020
IC19	SN74LS74N				510002600
IC20	SN74LS32N				510003140
IC21	SN74LS04N				510002690
IC22	SN74LS08N				510002910
IC23	SN74LS00N				510002000
IC24	SN74LS74N				510002600
IC25	SN74LS04N				510002690
IC26	SN74LS138N				510003530
IC31	SN74LS193N				510003580
IC32	SN74LS175				510003170
IC33	SN74LS175				510003170
IC34	SN74LS151N				510002720
IC35	SN74LS125N				510004630

PCB 1

Cct Ref.	General Description	Solartron Part No.
IC36	SN74LS138N	510003530
IC37	SN74LS244N	510004500
IC38	SN74LS244N	510004500
IC39	SN74LS362N	510004890
IC40	SN74LS138N	510003530
IC41	SN74LS138N	510003530
IC42	MK4118-3	510004730
IC43	MK4118-3	510004730
IC44	SN74LS74N	510002600
IC45	SN74S74N	510002020
IC46	SN74S37	510003330
IC47*	091E 0147	12005201AA
IC47	PAL16R4	510005360
IC48	SN74LS244N	510004500
IC49 to IC51	SN74LS244N	510004500
IC52	SN74LS138N	510003530
IC53	SN74LS138N	510003530
IC54	SN74LS30N	510003560
IC55	SN74LS374N	510004390
IC56	SN74LS244N	510004500
IC57	SN74S138N	510003400
IC58	MK4118-3	510004730
IC59	MK4118-3	510004730
IC60	SN74LS244N	510004500
IC61	SN74LS374N	510004390
IC62	SN74LS32N	510003140
IC63	SN74S30N	510003320
IC64	TMS9902 JL	510004930
IC65	AM26LS30	510004790
IC66	AM26LS32	510004800
IC67	SN74LS04	510002690
ZD1	Zener 5.1V	300521310
D1	SD3	300522160
D2	LED MV5024	300750060

PCB 1

Cct Ref.	General Description	Solartron Part No.
L1	Inductor 1µH	305020470
X1	Crystal 12MHz	300810750
PLA	Plug 64-way Eurocard	352364010
PLB	Plug 64-way Eurocard	352364010
PLC	Plug 32-way Eurocard	352332080
SW1	Switch DIL 8-way	375000600
SW2	Switch DPCO	375000510
SW3	Switch Toggle	376000880

PCB 2

Cct Ref.	General Description				Solartron Part No.
R1	MEOX	220	¼W	1%	195322200
R2 to R5	MEOX	1k	¼W	1%	195331000
R7	MEOX	1k	¼W	1%	195331000
R8	MEOX	1k	¼W	1%	195331000
RR9	MEOX	1.2k	¼W	1%	195331200
R10	MEOX	470	¼W	1%	195324700
R11	MEOX	560	¼W	1%	195425600
R12	MEOX	180	¼W	1%	195421800
R13	MEOX	47	¼W	1%	195614700
R14	MEOX	47	¼W	1%	195614700
R15	MEOX	75	¼W	1%	195317500
R16	MEOX	75	¼W	1%	195317500
R21	MEOX	100	¼W	1%	195321000
R23	MEOX	47	¼W	1%	195614700
R24	MEOX	47k	¼W	1%	195344700
R26	MEOX	100	¼W	1%	195321000
C1 to C3	TAND	10	20V	20%	265871000
C4 to C23	TAND	1	35V	20%	266061000
C24 to C56	CERM	.047		+50% -25%	241944700
C57	MICA	33p	350V	5%	250313300
C62	CERM	100p	500V	20%	241321000
C64	CERM	.047		+50% -25%	241944700
C69	CERM	330p	500V	+40% -20%	241323300
C70	TAND	10	20V	20%	265871000
C71 to C74	CERM	.047		+50% -25%	241944700

PCB 2

Cct Ref.	General Description				Solartron Part No.
C75	CERM	100p	500V	20%	241321000
TR1	BC107S				300553320
TR2	BC107S				300553320
TR3 to TR5	BCY70				300553590
IC1	SN74S00N				510003270
IC2	SN74S74N				510002020
IC3	SN74LS08N				510002910
IC4	SN74LS32N				510003140
IC5	SN74LS00N				510002000
IC6	SN74LS164N				510002890
IC7	SN74LS166N				510005070
IC8	SN74LS374				510004390
IC9 to IC12	MK4116				510004100
IC13	SN74S163N				510004260
IC14	SN74LS125N				510004630
IC15	SN74S04N				510002660
IC16	SN74LS74N				510002600
IC17	SN74LS74N				510002600
IC18	SN74LS74N				510002600
IC19	SN74LS14N				510003120
IC20	SN74LS166N				510005070
IC21	SN74LS374N				510004390
IC22 to IC25	MK4116				510004100
IC26	SN74S86N				510003360
IC27	SN74LS132				510002980
IC28	SN74LS374N				510004390
IC29	SN74LS138N				510003530
IC30	MK4118-1				510006080
IC31	MC6845				510005300
IC32	SN74LS00N				510002000
IC33	SN74LS74N				510002600

PCB 2

Cct Ref.	General Description	Solartron Part No.
IC34	SN74LS374N	510004390
IC35	SN74LS374N	510004390
IC36 to IC39	MK4116	510004100
IC40	SN74LS08N	510002910
IC41	SN74LS74N	510002600
IC42	SN74LS157	510003510
IC43	SN74LS245N	510004560
IC44	SN74LS244N	510004500
IC45	SN74LS244N	510004500
IC46	SN74LS08N	510002910
IC47	SN74LS138N	510003530
IC48	SN74LS374N	510004390
IC49	SN74LS374N	510004390
IC50 to IC53	MK4116	510004100
IC54	SN74LS175N	510003170
IC55	SN74LS08N	510002910
IC56	SN74LS00N	510002000
IC57	SN74LS00N	510002000
IC58	SN74LS125N	510004630
IC59	SN74LS125N	510004630
IC60	SN74LS244N	510004500
IC61	SN74S260	510004810
IC62	SN74LS20N	510002700
IC63	SN74LS173N	510004180
IC64	SN74LS244N	510004500
IC65	SN74LS244N	510004500
IC66	SN74LS374N	510004930
IC67	SN74LS244N	510004500
IC68	SN74LS374N	510004390
IC69	SN74LS244N	510004500
IC70	SN74LS123N	510002950
IC71	SN74S32N	510004240
IC72	SN74LS14N	510003120
IC73	SN74S175N	510003460

PCB 2

Cct Ref.	General Description	Solartron Part No.
ZD1	Zener BZY88 5.1V	300521310
D1 to D3	SD3	300522160
L1	Inductor 1μH	305020470
XL1	Crystal 22MHz	300810650
PLA	Plug 64-way Eurocard	352364010
PLB	Plug 64-way Eurocard	352364010
PLC	Plug 32-way Eurocard	352332080

PCB 3

Cct Ref.	General Description				Solartron Part No.
R1	MEOX	1k	¼W	1%	195431000
R2 to R8	MEOX	1k	¼W	1%	195331000
R9 to R12	CACP	15	¼W	10%	172011500
R13 to R15	MEOX	1k	¼W	1%	195331000
R16	MEOX	130	¼W	5%	195621300
C1 to C4	TAND	10	20V	20%	265871000
C5 to C15	CERM	.047		+50% -25%	241944700
C16	TAND	10	20V	20%	265871000
C17 to C36	CERM	.047		+50% -25%	241944700
IC1	SN74LS30				510003560
IC2	SN74LS138N				510003530
IC3	SN74LS74N				510002600
IC4	SN74LS74N				510002600
IC5	SN74LS74N				510002600
IC6	SN74LS32N				510003140
IC7	SN74LS74N				510002600
IC8	SN74LS138N				510003530
IC9	SN74LS195N				510004880
IC10	SN74LS138N				510003530
IC11*	E4BA 0311				12005205AA
IC11	2516				510003080
IC12*	7DB7 0312				12005204AA
IC12	2516				510003080
IC13	SN74LS125N				510004630
IC14	SN74LS04N				510002690
IC15	SN74LS138N				510003530
IC16	SN74LS08N				510002910

PCB 3

Cct Ref.	General Description	Solartron Part No.
IC17	SN74LS74N	510002600
IC18	SN74LS138N	510003530
IC19	SN74LS04N	510002690
IC20	MK4118	510004730
IC21	MK4118	510004730
IC22	SN74LS244N	510004500
IC23	SN74LS125N	510004630
IC24	TMS9900	510004920
IC25	SN74LS00N	510002000
IC26	SN74LS244N	510004500
IC27	SN74LS244N	510004500
IC28	SN74LS125N	510004630
IC29	SN74S74N	510002020
IC30	SN74LS164N	510002890
IC31	MK4118	510004730
IC32	MK4118	510004730
IC33	SN74LS245N	510004560
IC34	SN74LS245N	510004560
IC35	SN74LS125N	510004630
IC36	SN74LS244N	510004500
IC37	SN74LS245N	510004560
IC38	SN74LS245N	510004560
IC39	SN74LS03N	510004140
IC40	SN74LS161N	510004160
IC41	SN74LS362N	510004890
IC42*	21F9 0342	12005206AA
IC42	2516	510003080
IC43*	B41E 0343	12005207AA
IC43	2516	510003080
IC44	SN74LS00N	510002000
IC45	SN74LS74N	510002600
IC46	SN74LS74N	510002600
ZD1	Zener BZY88 5.1V	300521310
LED1	LED	300750060
TSKA	Socket 16-way DIL	300584900
PLA	Plug 64-way Eurocard	352364010
PLB	Plug 64-way Eurocard	352364010
SWA	Switch	375000510

PCB 4

Cct Ref.	General Description				Solartron Part No.
R1	MEOX	1k	¼W	1%	195331000
R2	MEOX	4.7k	¼W	1%	195334700
R3 to R12	MEOX	10k	¼W	1%	195341000
R15 to R24	MEOX	10k	¼W	1%	195341000
R25	MEOX	680	¼W	1%	195326800
R26 to R28	MEOX	4.7k	¼W	1%	195334700
R29	MEOX	680	¼W	1%	195326800
R30 to R37	MEOX	10k	¼W	1%	195341000
R39	MEOX	1k	¼W	1%	195331000
R40	MEOX	1.8k	¼W	1%	195331800
R41	MEOX	220	¼W	1%	195322200
R42	MEOX	1k	¼W	1%	195331000
C2	ESTF	33p	125V	10%	210213300
C3 to C9	TAND	10	20V	20%	265871000
C10 to C57	TAND	1.5	20V	20%	265861500
C58 to C105	CERM	.047		+50% -25%	241944700
C108 to C164	CERM	.047		+50% -25%	241944700
C170 to C178	CERM	.047		+50% -25%	241944700

PCB 4

Cct Ref.	General Description	Solartron Part No.
TR1	BC107	300553320
TR2	BCY70	300553590
TR3	2N4403	300555570
IC1 to IC6	MK4116-3	510004100
IC7 to IC13	MK4116-3	510004100
IC14 to IC20	MK4116-3	510004100
IC21 to IC48	MK4116-3	510004100
IC49	74LS374	510004390
IC50	74LS374	510004390
IC51	8202	510005270
IC52	74S241	510005090
IC53	74LS125	510004630
IC54	74LS04	510002690
IC55	74LS02	510002230
IC56	74LS00	510002000
IC57	74LS74	510002600
IC58	74LS32	510003140
IC59	74LS138	510003530
IC60	74LS32	510003140
IC61	74LS244	510004500
IC62	74LS244	510004500
IC63	74LS245	510004560
IC64	74LS245	510004560
IC65 to IC68	HM6514	510005400
IC69	74LS74	510002600
IC70	74LS157	510002240
IC71	74LS138	510003530
IC84	74LS14	510003120
IC85	74S00	510003270

PCB 4

Cct Ref.	General Description		Solartron Part No.
D1	Zener	5.1V	300521310
ZD2	Zener	4.3V	300523900
D3	SD3		300522160
L1	Inductor	1µH	305020470
X1	Crystal	25MHz	300810660
PLA	Plug 64-way Eurocard		352364010
PLB	Plug 64-way Eurocard		352364010
B1	Battery 2.4V		800400230
	Socket, DIL, 16 way (for IC1-IC48)		300584900
	Socket, DIL, 18 way (for IC65-IC68)		300585060
	Socket, DIL, 24 way (for IC72-IC83)		300584910

PCB 5

Cct Ref.	General Description				Solartron Part No.
R1 to R3	MEOX	330	¼W	5%	195623300
R4	MEOX	1k	¼W	5%	195631000
R5 to R19	MEOX	4.7k	¼W	5%	195634700
C1	TAND	10	20V	20%	265871000
C2 to C11	CERM	.047		+50% -25%	241944700
IC1	SN74LS245N				510004560
IC2	SN74LS245N				510004560
IC3	SN74LS138N				510003530
IC4	SN74LS138N				510003530
IC5	SN74LS244N				510004500
IC6*	091E 0506				12005201AA
IC6	PAL16R4				510005360
IC7	2940				510005330
IC8	2940				510005330
IC9	SN74LS11N				510003110
IC10	SN74LS74N				510002600
IC11	SN74LS00N				510002000
IC12	SN74LS02N				510002230
IC13	SN74LS32N				510003140
IC14	SN74LS08N				510002910
IC15	SN74LS04N				510002690
IC16	SN74LS74N				510002600
IC17	SN74LS74N				510002600
IC18	SN74LS08N				510002910
IC19	SN74LS125N				510004630
IC20	SN74LS161N				510004160
IC21	SN74LS138N				510003530
IC22	SN74LS32N				510003140
IC23	SN74LS74N				510002600
IC24	SN74LS157N				510002240
IC25	SN74LS08N				510002910
IC26	SN74LS32N				510003140

PCB 5

Cct Ref.	General Description	Solartron Part No.
IC27 to IC29	SN74LS244N	510004500
IC30	SN74LS273N	510004380
IC31	SN74LS74N	510002600
PLB	Plug 64-way Eurocard	352364010
PLC	Plug 50-way Right Angle	352350090
PLD	Plug 20-way Straight Entry	352320010
SKE	Socket, 24 way, DIL	300584910
	Stand-off insulator	412011020

PCB 6

Cct Ref.	General Description				Solartron Part No.
R1	MEOX	4.7k	¼W	5%	195634700
R2	MEOX	4.7k	¼W	5%	195634700
R3 to R5	MEOX	470	¼W	5%	195624700
C1 to C8	CERM	.047		+50% -25%	241944700
IC1	SN74LS257N				510002990
IC2	SN74LS257N				510002990
IC3	SN74LS373N				510004870
IC4	SN74LS373N				510004870
IC5	SN74LS04N				510002690
IC6	8291				510005590
IC7	8292				
IC8	SN74LS32N				510003140
IC9	SN74LS125N				510004630
IC10	SN74LS00N				510002000
IC11	SN74LS02N				510002230
IC12	SN74LS04N				510002690
IC13	SN74LS21N				510003130
IC14 to IC18	MC3448A				510004300
SKE	Socket 24-pin DIL				300584910
PLD	Plug 50-way Right Angle				352350090
	Header plug 24-way				351324060
	Plug 24-way, Right Angle				352326060

PCB 7

S1	Switch 8 x SPCO	375000540
S2	Switch 8 x SPCO	375000540

PCB 8

Cct Ref.	General Description				Solartron Part No.
R1 to R10	MEOX	1k	¼W	1%	195331000
R11 to R15	MEOX	10k	¼W	1%	195341000
R16	MEOX	330	¼W	1%	195323300
R17	MEOX	4.7k	¼W	1%	195334700
R18	MEOX	330	¼W	1%	195323300
R19	MEOX	330	¼W	1%	195323300
C1	TAND	10	20V	20%	265871000
C2	TAND	10	20V	20%	265871000
C3 to C50	CERM	.047		+50% -25%	241944700
C51	CERM	68p	500V	20%	241316800
IC1	SN74S00N				510003270
IC2	SN74S112N				510003370
IC3	SN74S112N				510003370
IC4	67401				510005460
IC5	SN74S241N				510005090
IC6	SN74S251N				510004910
IC7	SN74S138N				510003400
IC8	SN74S04N				510002660
IC9	SN74S251N				510004910
IC10	SN74S138N				510003400
IC11	SN74S32N				510004240
IC12	SN74LS169AN				510004850
IC13	SN74S00N				510003270
IC14	SN74S08N				510003300
IC15	SN74S20N				510002680
IC16	SN74S11N				510003310
IC17	SN74S138N				510003400
IC18	SN74S138N				510003400
IC19	SN74S374N				510005100
IC20	SN74S374N				510005100

PCB 8

Cct Ref.	General Description	Solartron Part No.
IC21	67401	510005460
IC22	SN74S241N	510005090
IC23	SN74S32N	510004240
IC24	SN74S00N	510003270
IC25	SN74S241N	510005090
IC26	SN74LS74N	510002600
IC27	SN74LS00N	510002000
IC28	SN74S02N	510003280
IC29	SN74S32N	510004240
IC30	SN74S20N	510002680
IC31	SN74S00N	510003270
IC32	SN74S10N	510002670
IC33	SN74S04N	510002660
IC34*	A7EA 0834	12005210BA
IC34	N82S191	510005450
IC35	SN74S374N	510005100
IC36	SN74LS244N	510004500
IC37	SN74LS244N	510004500
IC38	67401	510005460
IC39	SN74S74N	510002020
IC40	SN74S74N	510002020
IC41	SN74LS08N	510002910
IC42	SN74LS04N	510002690
IC43	SN74S74N	510002020
IC44	SN74LS161AN	510004160
IC45	SN74S74N	510002020
IC46	SN74S74N	510002020
IC47	SN74S08N	510003300
IC48	SN74S189N	510002840
IC49	SN74S175N	510003460
IC50	SN74S482N	510004940
IC51*	11E9 0851	12005211BA
IC51	N82S191	510005450
IC52 to IC54	SN74S374N	510005100
IC55	67401	510005460
IC56	SN74LS125N	510004630
IC57	SN74LS139N	510002960
IC58	SN74LS32N	510003140

PCB 8

Cct Ref.	General Description	Solartron Part No.
IC59	SN74LS30N	510003560
IC60	SN74LS00N	510002000
IC61	SN74LS161AN	510004160
IC62	SN74S153N	510003430
IC63	SN74S153N	510003430
IC64	SN74LS244N	510004500
IC65	SN74S189N	510002840
IC66	SN74S175N	510003460
IC67	SN74S482N	510004940
IC68*	F9E3 0868	12005212BA
IC68	N82S191	510005450
IC69	SN74S374N	510005100
IC70	SN74LS244N	510004500
IC71	SN74LS244N	510004500
IC72*	091E 0872	12005201AA
IC72	PAL16R4	510005360
IC73	SN74S374N	510005100
IC74	SN74S374N	510005100
IC75	SN74LS161AN	510004160
IC76	SN74LS161AN	510004160
IC77*	03CO 0877	12005208AA
IC77	74S288	
IC78*	1374 0878	12005209AA
IC78	745288	
IC79	SN74LS244N	510004500
IC80	SN74S189N	510002840
IC81	SN74S175N	510003460
IC82	SN74S482N	510004940
IC83*	FC7D	12005213BA
IC83	N82S191	510005450
IC84	SN74S374N	510005100
IC85	SN74LS10N	510002870
IC86	SN74LS259N	510004860
IC87	SN74S04N	510002660
IC88*	C186 0888	12005214BA
IC89*	11DC 0889	12005215BA
IC90*	FC28 0890	12005216BA
IC91*	A1FC 0891	12005217BA
IC88 to IC91	N82S191	510005450
IC92	SN74LS74N	510002600
IC93	SN74S241N	510005090

PCB 8

Cct Ref.	General Description	Solartron Part No.
D1	Diode MV5024	300750060
X1	Crystal 26.666MHz	300810680
L1	Inductor 0.47µH	305020620
PLA	Plug 64-way Eurocard	352364010
PLB	Plug 64-way Eurocard	352364010
PLC	Plug 32-way Eurocard	352332080
PLD	Header 40-way	352340020
PLE	Header 40-way	352340020
	Socket, DIL, 24 way	300584910

PCB 9

Cct Ref.	General Description				Solartron Part No.
R1 to R6	MEOX	1k	¼W	1%	195331000
R7 to R10	MEOX	100	¼W	1%	195321000
R11	MEOX	150	¼W	1%	195321500
R12	MEOX	1k	¼W	1%	195331000
C1	TAND	10	20V	20%	265871000
C2	TAND	10	20V	20%	265871000
C3 to C35	CERM	.047		+50% -25%	241944700
C36	CERM	33p	500V	20%	241313300
IC1	SN74S138N				510003400
IC2	SN74S04N				510002660
IC3	SN74S08N				510003300
IC4	SN74S02N				510003280
IC5 to IC7	SN74S153N				510003430
IC8	74S181N				510003470
IC9	SN74S00N				510003270
IC10	SN74S04N				510002660
IC11	SN74S00N				510003270
IC12	SN74S139N				510003410
IC13	MK4118A-3				510004730
IC14	MK4118A-3				510004730
IC15	SN74S374N				510005100
IC16	SN74S374N				510005100
IC17	AM29705				510005320
IC18	74S181N				510003470
IC19	SN74S30N				510003320
IC20	SN74S241N				510005090
IC21	SN74S32N				510004240
IC22	SN74S74N				510002020
IC23	SN74S74N				510002020
IC24	MK4118A-3				510004730

PCB 9

Cct Ref.	General Description	Solartron Part No.
IC25	MK4118A-3	510004730
IC26	SN74S374N	510005100
IC27	SN74S374N	510005100
IC28	AM29705	510005320
IC29	74S181N	510003470
IC30	SN74S260N	510004810
IC31	SN74S241N	510005090
IC32	SN74LS157N	510002240
IC33	SN74S74N	510002020
IC34	SN74S175N	510003460
IC35	SN74S11N	510003310
IC36	SN74S08N	510003300
IC37	SN74S138N	510003400
IC38	SN74S374N	510005100
IC39	SN74S374N	510005100
IC40	SN74S373N	510005110
IC41	AM29705	510005320
IC42	74S181N	510003470
IC43	SN74S182N	510003480
IC44	SN74S241N	510005090
IC45	SN74LS244N	510004500
IC46	SN74S74N	510002020
IC47	SN74S175N	510003460
IC48	SN74S32N	510004240
IC49	SN74S04N	510002660
IC50	SN74S138N	510003400
IC51	SN74S374N	510005100
IC52	SN74S00N	510003270
IC53	SN74S373N	510005110
IC54	AM29705	510005320
IC55	74S181N	510003470
IC56	SN74S260N	510004810
IC57	SN74S241N	510005090
IC58	SN74S251N	510004910
IC59	SN74S02N	510003280

PCB 9

Cct Ref.	General Description	Solartron Part No.
IC60 to IC63	MK4118A-3	510004730
IC64	SN74S00N	510003270
IC65	SN74S374N	510005100
IC66	SN74S02N	510003280
IC67	SN74LS373	510004870
IC68	SN74LS373	510004870
PLA	Plug 64-way Eurocard	352364010
PLB	Plug 64-way Eurocard	352364010
PLC	Plug 32-way Eurocard	352332080
	Socket, DIL, 28 way	300585160

PCB 10

Cct Ref.	General Description				Solartron Part No.
R1 to R3	MEOX	1k	¼W	1%	195331000
R4	MEOX	330	¼W	1%	195323300
R5	MEOX	1k	¼W	1%	195331000
R6	MEOX	330	¼W	1%	195323300
R7	MEOX	1k	¼W	1%	195331000
C1	TAND	10	20V	20%	265871000
C2	TAND	10	20V	20%	265871000
C3 to C48	CERM	.047		+50% -25%	241944700
C49	ESTF	100p	150V	10%	221321000
C50	ESTF	100p	150V	10%	221321000
IC1	SN74S10N				510002670
IC2	SN74S169N				510004270
IC3	SN74S04N				510002660
IC4	SN74LS273N				510004380
IC5	SN74S374N				510005100
IC6	SN74LS241N				510004370
IC7	SN74LS379				510005080
IC8	SN74S32N				510004240
IC9 to IC11	SN74S163N				510004260
IC12*	39B4 1012				12005221AA
IC12	DM74S74N				510005420
IC13*	4ABB 1013				12005222AA
IC13	DM74S74N				510005420
IC14	SN74S08N				510003300
IC15	SN74S04N				510002660
IC16*	006D 1016				12005218AA
IC16	82S129				510005430
IC17	SN74S283N				510004570
IC18	SN74S283N				510004570
IC19	SN74S257N				510003490
IC20	SN74LS241N				510004370
IC21	SN74S163N				510004260
IC22	SN74S138N				510003400
IC23	SN74S251N				510004910
IC24	SN74S74N				510002020

PCB 10

Cct Ref.	General Description	Solartron Part No.
IC25	SN74S00N	510003270
IC26	SN74S374N	510005100
IC27	MPY 16HJ	510005370
IC28	MPY 16HJ	510005370
IC29	SN74S32N	510004240
IC30	SN74S163N	510004260
IC31*	046D 1031	12005219AA
IC31	82S129	510005430
IC32	SN74S283N	510004570
IC33	SN74S283N	510004570
IC34	SN74S257N	510003490
IC35	SN74LS241N	510004370
IC36	SN74S163N	510004260
IC37	SN74S32N	510004240
IC38	SN74S04N	510002660
IC39	SN74S10N	510002670
IC40	SN74S00N	510003270
IC41	SN74S374N	510005100
IC42	SN74S374N	510005100
IC43	SN74S163N	510004260
IC44*	0492 1044	12005220AA
IC44	82S129	510005430
IC45	SN74S283N	510004570
IC46	SN74S283N	510004570
IC47	SN74S257N	510003490
IC48	SN74LS241N	510004370
IC49	SN74S163N	510004260
IC50	SN74S374N	510005100
IC51	SN74S138N	510003400
IC52	SN74S02N	510003280
IC53	SN74LS86N	510002880
IC54	SN74LS86N	510002880
IC55	SN74S169N	510004270
IC56	SN74S169N	510004270
IC57	SN74LS00N	510002000
IC58	SN74LS273N	510004380
IC59	SN74S374N	510005100
IC60	SN74S174N	510003450
IC61	SN74LS244N	510004500
IC62	SN74S374N	510005100

PCB 10

Cct Ref.	General Description	Solartron Part No.
IC63 to IC65	SN74S138N	510003400
IC66	SN74S174N	510003450
IC67	SN74S174N	510003450
IC68 to IC71	SN74S374N	510005100
IC72 to IC75	SN74S241N	510005090
IC76	SN74S374N	510005100
IC77	SN74S241N	510005090
IC78	SN74S241N	510005090
IC79	SN74S00N	510003270
IC80 to IC85	SN74S241N	510005090
IC86	SN74S74N	510002020
PLA	Plug 64-way Eurocard	352364010
PLB	Plug 64-way Eurocard	352364010
PLC	Plug 32-way Eurocard	352332080
PLD	Plug 40-way	352340020
PLE	Plug 40-way	352340020

PCB 11

Cct Ref.	General Description				Solartron Part No.
R1 to R8	MEOX	4.7k	¼W	1%	195334700
R9	MEOX	15k	¼W	1%	195341500
R10	MEFM	62k	¼W	0.5%	198246201
R11	MEFM	62k	¼W	0.5%	198246201
R12	MEOX	1.5k	¼W	1%	195331500
RV1	CMPS	10k	½W	10%	130441000
RV2	CMPS	10k	½W	10%	130441000
C1 to C3	TAND	10	20V	20%	265871000
C4 to C13	CERM	.047		+50% -25%	241944700
C15	ESTF	100n	100V	10%	225451000
C16 to C20	CERM	.047		+50% -25%	241944700
C24	STYR	180p	125V	10%	210221800
TR1	BC107				300553320
IC1	SN74LS125N				510004630
IC2	SN74LS32N				510003140
IC3	SN74LS174N				510002970
IC4	SN74LS175N				510003170
IC5	SN74LS174N				510002970
IC6	SN74LS175N				510003170
IC7	SN74LS244N				510004500
IC8	SN74LS04N				510002690
IC9	SN74LS21N				510003130
IC10	SN74LS32N				510003140
IC11	SN74LS138N				510003530
IC12	SN74LS175N				510003170
IC13	SN74LS08N				510002910
IC14	SN74121N				510000530
IC15	SN74LS74N				510002600
IC16	SN74S161N				510004160
IC17	RELAY DIL 121A-3				300652000

PCB 11

Cct Ref.	General Description	Solartron Part No.
IC18	DAC-03 DIL	550001200
IC19	DAC-03 DIL	550001200
IC20	SN74LS74N	510002600
D1	SD3	300522160
L1	Inductor 1μH	305020470
X1	Crystal, 12MHz	300810750
SW1	Switch 16-pin DIL	375000620
RL1	Relay NF2-6V	300652140
SKA	Socket 15-way Cannon	352515060
PLB	Plug 64-way Eurocard	352364010

PCB 18

Cct Ref.	General Description	Solartron Part No.
SKA		
SKB	Socket 64-way Eurocard	352364010
SKC		
PLA	Plug 64-way Eurocard	352564010

PCB 19

Cct Ref.	General Description				Solartron Part No.
R1 to R16	MEOX	2.2k	¼W	1%	195332200
R17	MEOX	1k	¼W	1%	195331000
R18	MEOX	1k	¼W	1%	195331000
R19 to R34	MEOX	2.2k	¼W	1%	195332200
R35	MEOX	1k	¼W	1%	195331000
R36	MEOX	470	¼W	1%	195324700
R37	MEOX	220	¼W	1%	193522200
R38	MEOX	330	¼W	1%	195323300
IC1	MC 12-470/5				550001270
IC2	MC 12-470/5				550001270
SKA1 to SKA15	Socket 64-way Eurocard				352564010
SKB1 to SKB16	Socket 64-way Eurocard				352564010
SKC5 to SKC9	Socket 32-way Eurocard				352532360
SKC11	Socket 32-way Eurocard				352532360
SKC14	Socket 32-way Eurocard				352532360
SKD	Plug 26-way				352326100
SKE	Socket Coax right angle				352101530
SKF	Socket Coax right angle				352101530
SKG	Socket Coax right angle				352101530
SKH	Socket Coax straight				352101510
PLA	Plug 10-way 220/1550				362310090
PLB	Berg St 36-way				362336080

PCB 20

Cct Ref.	General Description				Solartron Part No.
R1 to R5	MEOX	4.7k	¼W	1%	195334700
R6 to R9	MEOX	1k	¼W	1%	195331000
R10 to R13	MEOX	4.7k	¼W	1%	195334700
R14	MEOX	2.2k	¼W	1%	195332200
R15	MEOX	1k	¼W	1%	195331000
R16	MEOX	1k	¼W	1%	195331000
R17		220k			
C1	TAND	10	20V	20%	265871000
C2	TAND	10	20V	20%	265871000
C3 to C24	CERM	.047		+50% -25%	241944700
C25	TAND	10	20V	20%	265871000
IC1	SN74LS00N				510002000
IC2	SN74LS04N				510002690
IC3	SN74LS08N				510002910
IC4	SN74LS74N				510002600
IC5	SN74LS74N				510002600
IC6	UA9636				
IC7	SN74S289N				510005540
IC8	SN74LS157AN				510002240
IC9	2716				510003080
IC10	SN74LS04N				510002690
IC11	SN74LS00N				510002000
IC12	SN74LS74N				510002600
IC13	SN74LS193N				510003580
IC14	SN74LS175N				510003170
IC15	SN74LS30N				510003560
IC16	UA9637				

PCB 20

Cct Ref.	General Description	Solartron Part No.
IC17	SN74LS74N	510002600
IC18	SN74S289N	510005540
IC19	SN74LS157N	510002240
IC20	2716	510003080
IC21	SN74LS151N	510002720
IC22	SN74LS74N	510002600
IC23	SN74LS193N	510003580
IC24	SN74LS10N	510002870
IC25	SN74LS138N	510003530
IC26	TMS9902JL	510004930
IC27	SN74LS74N	510002600
IC28	SN74S289N	510005540
IC29	SN74LS157N	510002240
IC30	2716	510003080
IC31	SN74LS74N	510002600
IC32	SN74LS00N	510002000
IC33	SN74LS175N	510003170
IC34	SN74LS193N	510003580
IC35	SN74LS244N	510004500
IC36	SN74LS138N	510003530
IC37	SN74LS04N	510002690
IC38	SN74LS175N	510003170
IC39	SN74S289N	510005540
IC40	SN74LS174N	510002970
IC41	2716	510003080
IC42	SN7407N	510000750
IC43	SN74LS02N	510002230
IC44	SN74LS244N	510004500
IC45	SN74LS193N	510003580
IC46	SN74LS244N	510004500
IC47	SN74LS11N	510003110
IC48	SN74LS30N	510003560
IC49 to IC53	SN74LS244N	510004500
IC54	SN74LS74N	510002600

PCB 20

Cct Ref.	General Description	Solartron Part No.
D1	LED	300750060
SW1	Switch SPCO	376000880
SW2	Switch SPCO	376000880
SW3	Switch DIL 4PST	375000640
SW4	Switch SPCO	376000880
SKA	Socket 25-way Cannon	352525040
PLA	Plug Eurocard	352364010
PLB	Plug Eurocard	352364010
PLD	Plug 40-way	352340020
PLE	Plug 40-way	352340020

PCB 21

SKA	Socket 40-way				300584970

PCB 22

SKA	Socket 40-way				300584970

PCB 23

R1	MEOX	4.7k	¼W	1%	195334700
R2	MEOX	4.7k	¼W	1%	195334700
R3	MEOX	1k	¼W	1%	195331000
R4 to R7	MEOX	330	¼W	1%	195323300
R8	MEOX	1k	¼W	1%	195331000
R9 to R12	MEOX	4.7k	¼W	1%	195334700
R13	MEOX	1k	¼W	1%	195331000
C1	TAND	10	20V	20%	265871000
C2 to C24	CERM	.047		+50% -25%	241944700

PCB 23

Cct Ref.	General Description	Solartron Part No.
IC1	SN74LS244N	510004500
IC2	SN74LS244N	510004500
IC3	SN74S74N	510002020
IC4	SN74LS273N	510004380
IC5	SN74S74N	510002020
IC6	SN74S20N	510002680
IC7	SN74LS191N	510004190
IC8	SN74S289N	510005540
IC9	SN74S157N	510003510
IC10	SN74LS244N	510004500
IC11 to IC18	C2417	510005560
IC19	SN74S02N	510003280
IC20	SN74S74N	510002020
IC21	SN74LS244N	510004500
IC22	SN74LS244N	510004500
IC23	SN74S74N	510002020
IC24	SN74S30N	510003320
IC25	SN74LS191N	510004190
IC26	SN74LS289N	510005540
IC27	SN74S157N	510003510
IC28	SN74LS244N	510004500
IC29 to IC36	C2417	510005560
IC37	SN74LS32N	510003140
IC38	SN74S74N	510002020
IC39	SN74LS244N	510004500
IC40	SN74LS374N	510004390
IC41	SN74S74N	510002020
IC42	SN74LS244N	510004500
IC43	SN74LS191N	510004190
IC44	SN74S289N	510005540

PCB 23

Cct Ref.	General Description	Solartron Part No.
IC45	SN74S157N	510003510
IC46	SN74LS244N	510004500
IC47 to IC54	C2417	510005560
IC55	SN74S260N	510004810
IC56	SN74S74N	510002020
IC57	SN74LS244N	510004500
IC58	SN74LS244N	510004500
IC59	SN74S74N	510002020
IC60	SN74LS244N	510004500
IC61	SN74LS191N	510004190
IC62	SN74LS244N	510004500
IC63	SN74LS244N	510004500
IC64	SN74LS244N	510004500
IC65 to IC72	C2147	510005560
IC73	SN74LS161AN	510004160
IC74	SN74LS10N	510002870
IC75	SN74LS04N	510002690
IC76	SN74LS244N	510004500
IC77	SN74S00N	510003270
IC78	SN74LS138N	510003400
IC79	SN74LS138N	510003530
IC80	SN74LS138N	510003530
IC81	SN74S08N	510003300
IC82 to IC85	SN74S374N	510005100
IC86	SN74LS244N	510004500
IC87	SN74LS273N	510004380
IC88	SN74LS151N	510004720
IC89	SN74LS244N	510004500

PCB 23

Cct Ref.	General Description	Solartron Part No.
IC90	SN74LS244N	510004500
IC91	SN74LS125N	510004630
IC92	SN74LS30N	510003560
IC93	SN74LS02N	510002230
IC94	SN74LS04N	510002690
IC95	SN74S241N	510005090
IC96	SN74S241N	510005090
IC97	SN74S00N	510003270
PLA	Plug 64-way Eurocard	352364010
PLB	Plug 64-way Eurocard	352364010
PLC	Plug 32-way Eurocard	352332080
PLD	Plug 40-way Sci Flex	352340020
PLE	Plug 40-way Sci Flex	352340020
PLF	Plug 40-way Sci Flex	352340020

PCB 25

Cct Ref.	General Description	Solartron Part No.
SKA	Socket 64-way Eurocard	352564040
SKB	Socket 64-way Eurocard	352564040
SKC	Socket 32-way Eurocard	352532380
PLA	Plug 64-way Eurocard	352364010
PLB	Plug 64-way Eurocard	352364010
PLC	Plug 32-way Eurocard	352332080

PCB 26

Cct Ref.	General Description	Solartron Part No.
SKA	Socket 64-way Eurocard	352564010
SKB	Socket 64-way Eurocard	352564010
SKC	Socket 32-way Eurocard	352532360
PLA	Plug 64-way Eurocard	352364010
PLB	Plug 64-way Eurocard	352364010
PLC	Plug 32-way Eurocard	352332080

PCB 27

Cct Ref.	General Description	Solartron Part No.
SKA	Socket 64-way Eurocard	352564010
PLA	Plug 64-way Eurocard	352364010

PCB 28

Cct Ref.	General Description				Solartron Part No.
R1	MEOX	1k	¼W	1%	195331000
R2	MEOX	470	¼W	1%	195324700
R3	MEOX	1k	¼W	1%	195331000
R4	MEOX	470	¼W	1%	195324700
R5 to R7	MEOX	1k	¼W	1%	195331000
C1	TAND	10	20V	20%	265871000
C2	TAND	10	20V	20%	265871000
C3 to C22	CERM	.047		+50% -25%	241944700
TR1	2N4403				300555570
TR2	2N4403				300555570
IC1*	39B1	2801			12005240DA
IC2*	E846	2802			12005241DA
IC3*	46D9	2803			12005242DA
IC4*	65A6	2804			12005243DA
IC5*	580A	2805			12005244DA
IC6*	CE81	2806			12005245DA
IC7*	A05A	2807			12005246DA
IC8*	58CA	2808			12005247DA
IC9*	9E91	2809			12005248DA
IC10*	7159	2810			12005249DA
IC11*	9B4E	2811			12005250DA
IC12*	03F7	2812			12005251DA
IC13*	92F5	2813			12005252DA
IC14*	E167	2814			12005253DA
IC15*	NOT USED				12005254D
IC16*	NOT USED				12005255D
IC17*	375F	2817			12005256DA
IC18*	6F4A	2818			12005257DA
IC19*	88C2	2819			12005258DA
IC20*	F4DC	2820			12005259DA
IC21*	E991	2821			12005260DA
IC22*	2F56	2822			12005261DA
IC23*	9C1D	2823			12005262DA
IC24*	EC83	2824			12005263DA

PCB 28

Cct Ref.	General Description	Solartron Part No.
IC1 to IC24	2532JL	510004530
IC25	SN74S04N	510002660
IC26	SN74LS244N	510004500
IC27	SN74LS244N	510004500
IC28	SN74LSN374	510004390
IC29	SN74LS244N	510004500
IC30	SN74LS244N	510004500
IC31 to IC33	SN74S138N	510003400
IC34	SN74S30N	510003320
IC35	SN74S30N	510003320
IC36	SN74S02N	510003280
IC37	SN74LS32N	510003140
IC38 to IC41	SN74LS157N	510002240
PLA	Plug 64-way Eurocard	352364010
PLB	Plug 64-way Eurocard	352364010

RVC Front Panel

Cct Ref.	General Description	Solartron Part No.
	Brilliance control:	
	CAFS 2.2M 20%	110025170
	Thumbwheel	12002003A
	Cable, CRT assy to motherboard	12000229A
	Contrast control:	
	CAFS 100 20%	110025160
	Thumbwheel	12002003A
	CRT assembly	5596014-01
	comprising:	
	VP1008 horizontal timebase	
	VP1101 line output (eht)	
	VP1200 video amplifier	
	VP1300 vertical timebase	
	VP1400 scanning yoke	
	9007 CRT M 23/17GR cathode ray tube	
	CRT earth lead	12000235A
	Eurocard socket, 64 way	352564020
	Keyboard interface	12100553X
	Main keyboard (below display)	12100106A
	comprising:	
	switch panel	12100205X
	keyboard moulding	12002030A
	M4 full nuts (8 off)	410031020
	M4 spring washers (8 off)	411320020
	M4 plain washers (8 off)	411029020
	Power switch assembly	12000230A
	Ribbon cable, keyboard interface to motherboard.	12000224A
	Ribbon cable, softkeys to keyboard interface	12000225A
	Softkey assembly,	12000115A
	comprising:	
	switch panel	12000210A
	switch moulding	12002022A
	M4 full nuts (4 off)	410031020
	M4 crinkle washers (4 off)	411129020
	Earth lead	12100211A
	Keyswitch Assembly	12100210A

RVC Mainframe

Cct Ref.	General Description	Solartron Part No.
	Ac supply connector	550001230
	Ac supply cableform	12000227B
	Capacitor, ALME 2,200 40V	273892200
	Dc supply cableform	12000226A
	Fan, 240V	380110260
	Fuse holder	360106030
	Fuse link, Slow-blow	
	1.6A (230V operation)	360106330
	3.15A (115V operation)	360206210
	Mains selector switch	375000590
	Mains transformer	12000236A
	12V power supply	550001250
	5V power supply	550001260
	Terminal block	355604050
	Resistor, 1M	172361000
	Earth lead 1 (to fan)	12000240A
	Earth lead 2 (to fan)	12000241A

RVC Input Connector Panel

Cct Ref.	General Description	Solartron Part No.
	BNC Socket	352101280
	in six positions, fitted with:	
	plastic bush	470120110
	pvc washer	12002042A
	solder tag	355700370
	Sub-minature connector	
	(Charge Input)	352101550
	Cable assembly, 25 way	12000223A
	(Serial link)	
	Cable assembly, 25 way	12100209X
	(Interlock)	
	Coaxial cables:	
	Voltage Hi	12100218X
	Voltage Lo	12100214X
	Generator Hi	12100217X
	Generator Lo	12100216X
	Generator Monitor	12100215X
	Video	12100208X
	Charge	12100207X

RVC Accessories

Cct Ref.	General Description	Solartron Part No.
	Connector, Cannon, 15 way, for analogue plotter, comprising:	
	plug, solder, 15 way	351315040
	shell, right angled	354004470
	slide lock	354004460
	Fuse links, 1.6A & 3.15A (as shown above)	
	Mains lead:	
	U.K.	359900380
	Europe	359900250
	USA and Canada	359900390
	Other countries	480140220
	Rack mounting ears	12002033A

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Cct Ref.	General Description				Solartron Part No.
R1	MEOX	220	1/4W	1%	195322200
R2	MEOX	220	1/4W	1%	195322200
R3 to R18	MEOX	1k	1/4W	1%	195331000
C1	TAND	20	20V	20%	265872000
C2	TAND	20	20V	20%	265872000
C8 to C48	CERM	.047	25V	20%	241944700
CV1		5.5-60p			290030190
IC1	SN74LS30				510003560
IC2	SN74LS27				510004150
IC3	SN74LS74				510002600
IC4	SN74LS74				510002600
IC5	SN74LS04				510002690
IC6	SN74LS00				510002000
IC7	SN74LS00				510002000
IC8	SN74LS125A				510004630
IC9	SN74LS02				510002230
IC10	PAL16R4				510005360
IC11	SN74LS138				510003530
IC12	SN74LS138				510003530
IC13	SN74LS157				510002240
IC14	AM2940				510005330
IC15	AM2940				510005330
IC16	SN74LS74				510002600
IC17	SN74LS08				510002910
IC18	SN74LS244				510004500
IC19	SN74LS244				510004500
IC20	SN74LS273				510004380
IC21	SN74LS74				510002600
IC22	SN74LS32				510003140
IC23	SN74LS00				510002000
IC24 to IC27	SN74LS74				510002600
IC28	SN74LS161A				510004160
IC29	SN74LS161A				510004160
IC30	SN74LS273				510004380
IC31	SN74LS161A				510004160
IC32	SN74LS273				510004380
IC33	SN74LS161A				510004160

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Cct Ref.	General Description	Solartron Part No.
IC34	SN74LS161A	510004160
IC35	SN74LS74	510002600
IC36	SN74LS08	510002910
IC37	SN74LS08	510002910
IC38	SN74LS32	510003140
IC39	SN74LS32	510003140
IC40	SN74LS08	510002910
IC41	SN74LS00	510002000
IC42	SN74LS112	510005000
IC43	SN74LS112	510005000
IC44	SN74LS390	510004410
IC45	SN74LS393	510004470
IC46	SN74LS244	510004500
IC47	SN74LS244	510004500
IC48	SN74LS74	510002600
IC49	SN74LS00	510002000
IC50	SN74LS273	510004380
IC51	SN74LS85	510002930
IC52	SN74LS161A	510004160
IC53	SN74LS74	510002600
IC54	SN74LS74	510002600
IC55	SN74LS139	510002960
IC56	SN74LS00	510002000
IC57	SN74161A	510004160
IC58	SN74LS273	510004380
IC59	SN74LS244	510004500
IC60	SN74LS08	510002910
X1	Crystal, 16.128MHz	
PLA	Plug, Eurocard	352364010
PLB	Plug, Eurocard	352364010

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Cct Ref.	General Description				Solartron Part No.
R1	MEFM	18k	1/8W	0.5%	192741802
R2	MEFM	1M	1/4W	0.1%	198361002
R3	MEFM	1M	1/4W	0.1%	198361002
R4	MEFM	330k	1/4W	0.1%	198153304
R5	MEFM	3.3k	1/8W	0.5%	192733302
R6	MEFM	330k	1/4W	0.1%	198153304
R8	MEFM	1.2k	1/8W	0.5%	192731202
R9	MEOX	47	1/4W	5%	195614700
R10	MEOX	47	1/4W	5%	195614700
R11	MEFM	10M	1W	1%	198971002
R12	MEFM	10M	1W	1%	198971002
R13	MEFM	2k	1/4W	0.1%	198132001
R14	MEFM	220k	1/8W	0.5%	192752202
R15	MEOX	47	1/4W	5%	195614700
R16	MEOX	47	1/4W	5%	195614700
R17	MEFM	100k	1/8W	0.5%	192751002
R18	MEFM	30k	1/4W	0.5%	198243001
R19	MEFM	2.7k	1/8W	0.5%	192732702
R20	MEOX	47	1/4W	5%	195614700
R21	MEOX	47	1/4W	5%	195614700
R22	MEFM	1.5k	1/4W	0.1%	160400347
R23	MEFM	10k	1/8W	0.5%	192741002
R24	MEOX	47	1/4W	5%	195614700
R25	MEOX	47	1/4W	5%	195614700
R26	MEFM	10k	1/8W	0.5%	192741002
R27	MEOX	12k	1/4W	1%	195341200
R28	MEOX	12k	1/4w	1%	195341200
R29	MEOX	1k	1/4W	1%	195331000
R30	MEOX	1k	1/4W	1%	195331000
R31	MEOX	12k	1/4W	1%	195341200
R32	MEOX	8.2k	1/4W	5%	195638200
R33	MEOX	8.2k	1/4W	5%	195638200
R40	MEFM	3.3k	1/8W	0.5%	192733302
R41	MEOX	1k	1/4W	1%	195331000
R42	MEFM	2.7	1/4W	1%	198302702
R46	MEFM	15k	1/8W	0.5%	192741501
R47	MEFM	10k	1/8W	0.5%	192741002
R48	MEFM	2.4k	1/4W	0.1%	198132401
R49	MEFM	2.5k	1/4W	1%	192932501
R51 to R54	MEFM	2k	1/4W	0.1%	198132001

PCB 52 Cct Ref.	General Description				Solartron Part No.
C84 to C86	CERM	.047	25V	+50% -20%	241944700
C87	TAND	0.47			266054700
C88	TAND	0.47			266054700
C89	ESTM	0.22	160V	10%	220052200
C90	CERM	.047	25V	+50% -20%	241944700
C91 to C93	TAND	10	20V	20%	265871000
C94 to C97		100p			241321000
IC1 to IC3	OP15F				510091150
IC4	HI 201-5/ADC /201 CI				510090930
IC5	AD 7533				510090670
IC6	OP15F				510091150
IC7	AD 7533				510090670
IC8	OP15F				510091150
IC9	OP15F				510091150
IC10	LM339				510090490
IC11	SN74LS374N				510004390
IC12	SN74LS374N				510004390
IC13	AD583/HA242J				510090920
IC14	ADC80				550001460
IC15	SN74LS374N				510004390
IC16	SN74LS374N				510004390
IC17	SN74LS244N				510004500
IC18	SN74LS244N				510004500
IC20 to IC22	SN74LS04N				510002690
IC23	SN7407N				510000750
IC24	SN74LS42N				510002710
IC26	SN74LS00N				510002000
IC27	REF 02 HP				510090940
IC28	MCD 15-190				550001240
IC29	KEMO 2171				559601601

PCB 52

Cct Ref.	General Description	Solartron Part No.
IC30	SN74LS374N	510004390
IC31	SN74LS374N	510004390
IC32	SN74LS273	510004380
IC33 to IC35	SN74LS374N	510004390
IC35		
IC36	AD 7533	510090670
IC37	AD 7533	510090670
IC38	REF 01	510091390
IC39	OP15F	510091150
IC40	OP15F	510091150
IC41	DAC 9331-16-5	510091380
IC42	OP15F	510091150
IC43	OP15F	510091150
IC45	KEMO 2171	559601601
IC46 to IC48	OP15F	510091150
D1 to D4	PAD10	300525340
D5 to D9	SD3	300522160
RLA to RLD	Reed Relay RS-5	300652030
PLA	Plug Eurocard 64/96	352364010
PLB	Plug Eurocard 64/96	352364010
SK1 to SK4	Connector	352304070
	Socket, 32 pin DIL	300585260
	Socket, 24 pin DIL	300584910
	Test Hooks	355400760

PCB 52

Cct Ref.	General Description				Solartron Part No.
R55	MEFM	1.5k	1/4W	0.1%	160400347
R56	MEFM	1.5k	1/4W	0.1%	160400347
R57 to R60	MEFM	2.4k	1/4W	0.1%	198132401
R61	MEFM	300	1/4W	0.1%	198123004
R62	MEFM	300	1/4W	0.1%	198123004
R63 to R66	MEFM	10k	1/8W	0.5%	192741002
R67	MEFM	2.7	1/4W	1%	198302702
R68	MEFM	1M	1/4W	0.1%	198361002
R69	MEFM	560	1/8W	0.5%	192725604
RV1	CMPM	5k	1/2W	10%	130635000
RV2	CMPM	2k	1/2W	10%	130632000
RV3	CMPM	10k	1/2W	10%	130641000
RV4		100k	1/2W	10%	130951000
RV5		100k	1/2W	10%	130951000
RV6	CMPM	5k	1/2W	10%	130635000
RV7	CMPM	5k	1/2W	10%	130635000
RV8		100k	1/2W	10%	130951000
RV11		100k	1/2W	10%	130951000
RV16		5k	1/2W	20%	130935000
RV17		100k	1/2W	10%	130951000
RV18		100k	1/2W	10%	130951000
RV19		200	1/2W		130922000
RV20		100k	1/2W	10%	130951000
RV21		100k	1/2W	10%	130951000
RV23 to RV25		100k	1/2W	10%	130951000
C1	ESTM	0.22	160V	10%	220052200
C2		0.2-2p	600V		290060100
C3		0.2-2p	600V		290060100
C4	MICA	3p	350V	1.7%	208500068
C6	CERM	.047	25V	+50% -20%	241944700
C7	CERM	.047	25V	+50% -20%	241944700
C8	MICA	1000p	125V	1%	208500057
C9	MICA	1000p	125V	15	208500057

PCB 52

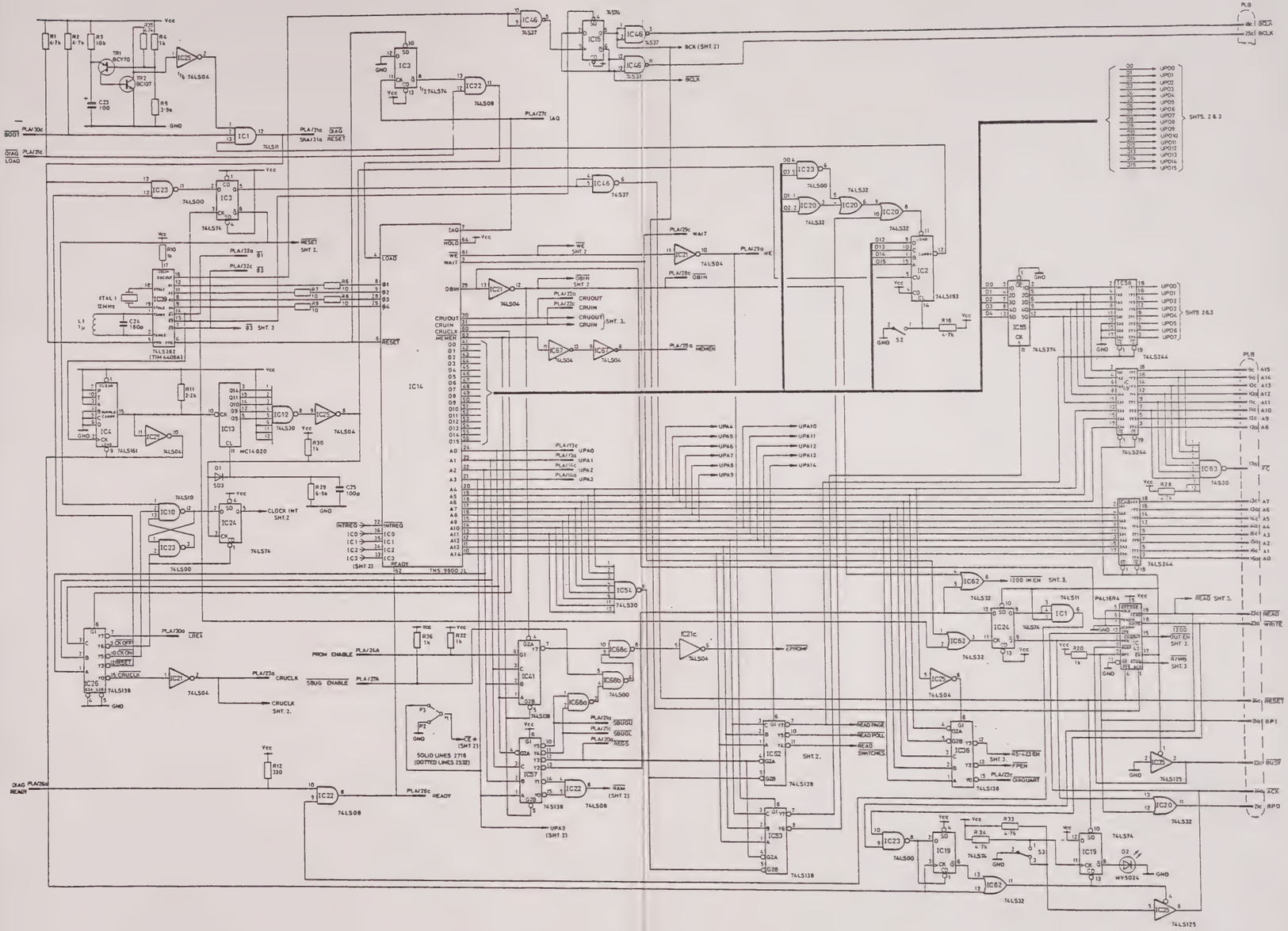
Cct Ref.	General Description				Solartron Part No.
C10	CERM	.047	25V	+50% -20%	241944700
C11	CERM	.047	25V	+50% -20%	241944700
C13	CERM	150p	500v	20%	241321500
C14 to C17	CERM	.047	25V	+50% -20%	241944700
C18	STYR	330p	125V	2.5%	210123300
C19	STYR	330p	125V	2.5%	210123300
C20 to C32	CERM	.047	25V	+50% -20%	241944700
C34 to C47	CERM	.047	25V	+50% -20%	241944700
C50	MICA	2200p	350V	5%	250332200
C51 to C55	TAND	10	20V	20%	265871000
C56	CERM	.047	25V	+50% -20%	241944700
C57	ESTM	0.22	160V	10%	220052200
C58	CERM	.047	25V	+50% -20%	241944700
C59	CERM	.047	25V	+50% -20%	241944700
C61	TAND	1			266061000
C62	CERM	.047	25V	+50% -20%	241944700
C69	CERM	.047	25V	+50% -20%	241944700
C70 to C72	CERM	.047	25V	+50% -20%	241944700
C73	TAND	1			266061000
C74	CERM	.047	25V	+50% -20%	241944700
C82	CERM	.047	25V	+50% -20%	241944700
C83	TAND	10	20V	20%	265871000

PCB 53

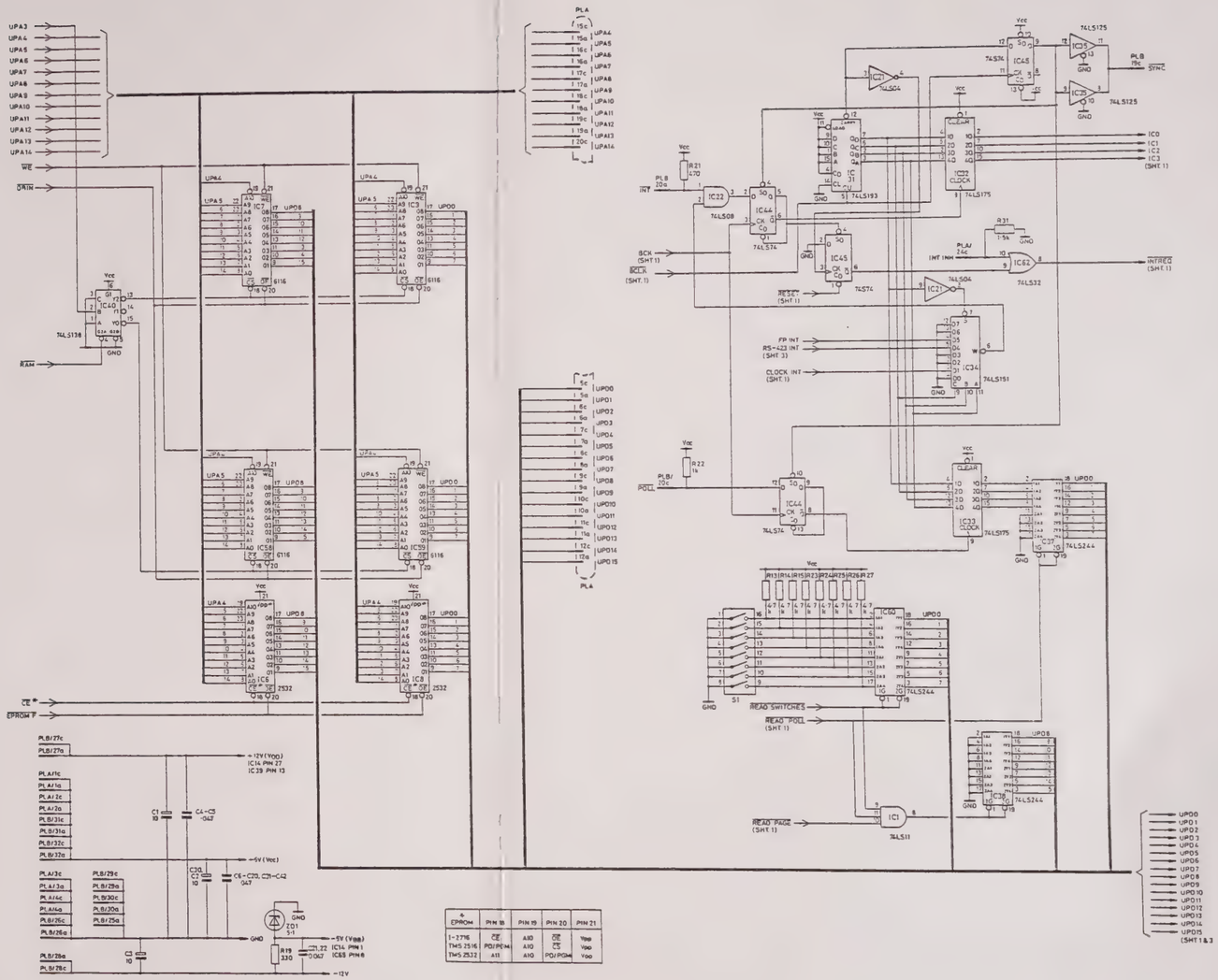
Cct Ref.	General Description				Solartron Part No.
R1	MEOX	47k	1/4W	5%	195644700
R2	MEOX	5.6k	1/4W	5%	195635600
R3	MEOX	47k	1/4W	5%	195644700
R4	MEOX	47k	1/4W	5%	195644700
R5	MEOX	10	1/4W	5%	195611000
R6	MEOX	47k	1/4W	5%	195644700
R7	MEOX	5.6k	1/4W	5%	195635600
R8	MEOX	82k	1/4W	5%	195648200
R9	MEOX	330	1/4W	5%	195623300
R10	MEOX	82k	1/4W	5%	195648200
R11	MEOX	10k	1/4W	5%	195641000
R12	MEOX	10k	1/4W	5%	195641000
R13	MEOX	15k	1/4W	5%	195341500
R14	MEOX	220	1/4W	5%	195622200
R15	MEOX	680	1/4W	5%	195626800
R16	MEOX	1k	1/4W	5%	195631000
R17	MEOX	5.6k	1/4W	5%	195635600
R18	MEOX	5.6k	1/4W	5%	195635600
R19	MEOX	10k	1/4W	5%	195641000
R20		22k			195342200
RV1	CAPS	4.7k	1/2W	5%	137434700
C1 to C24	CERM	.047	20V	20%	241944700
C25	ESTF	100p	160V	10%	221321000
C26	ESTM	0.1	160V	10%	220351000
C27	ESTF	100p	160V	10%	221321000
C28	TAND	4.7	35V	20%	266064700
C29	ESTF	100p	160V	10%	221321000
C30	CERM	47p	500V	20%	241314700
C31	TAND	1	35V	20%	266061000
C32	ESTF	470p	400V	10%	222324700
C33 to C35	TAND	10	35V	10%	265871000
C36	CERM	.047	20V	20%	241944700
IC1	KR-3600-PRO				510005340
IC2	AY-5-1013A				510002540
IC3	SN74LS74N				510002600
IC4	SN74LS74N				510002600

PCB 53

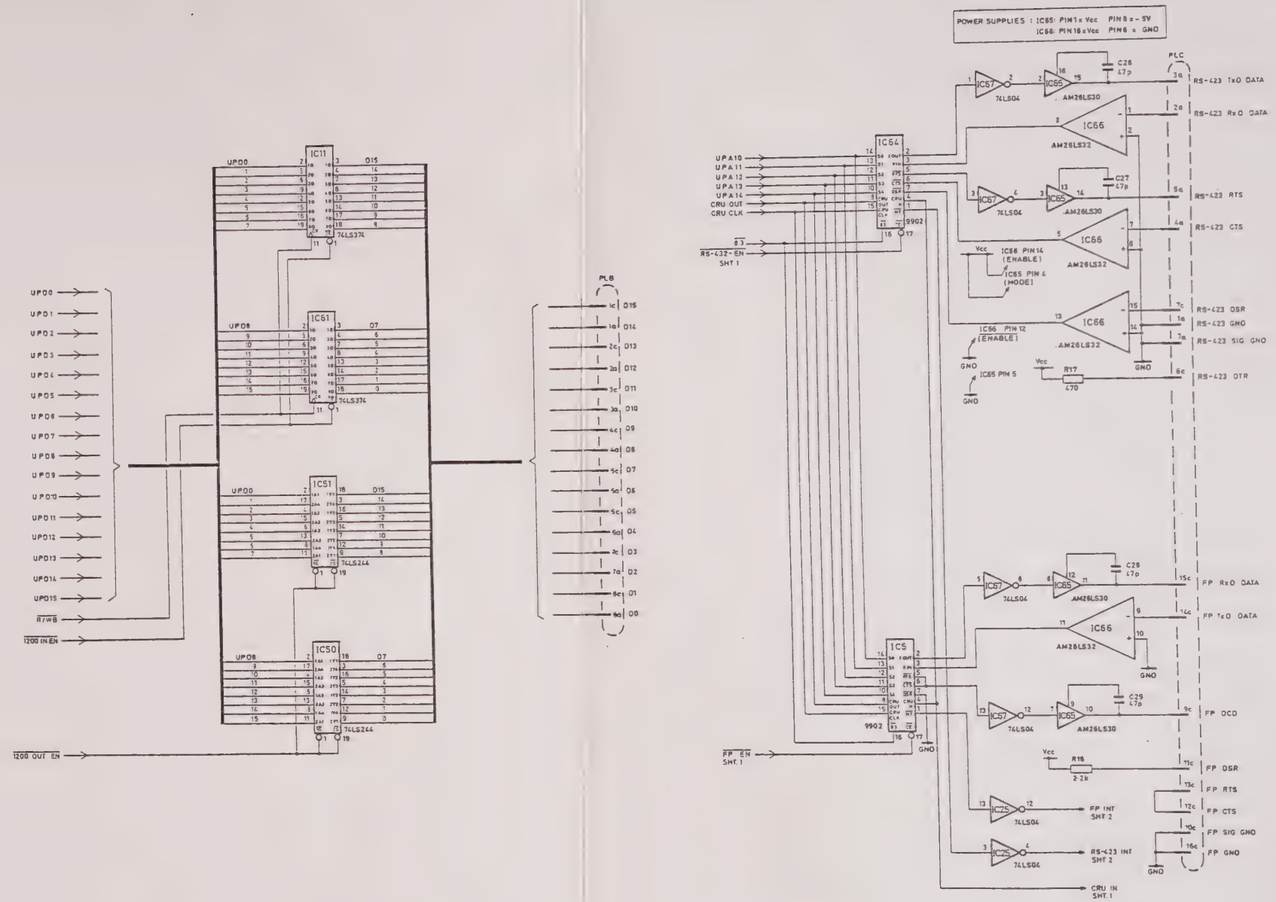
Cct Ref.	General Description	Solartron Part No.
IC5	SN74LS157N	510002240
IC6	SN74LS85N	510002930
IC7	SN74LS123N	510002950
IC8	SN74LS123N	510002950
IC9	555	510006260
IC10	AM26LS32	510004800
IC11	AM26LS30	510004150
IC12	SN74LS27N	510004790
IC13	SN74LS32N	510003140
IC14	SN74LS08N	510002910
IC15	SN74LS04N	510002690
IC16	SN7406N	510000760
TR1	BC107	300553320
TR2	BCY70	300553590
TR3	BCY70	300553590
D1 to D4	SD3	300522160
ZD1	Zener diode 5V1	300521310
ZD2	Zener diode 5V1	300521310
LED1	LED (red)	300750080
OPTO 1	Opto coupler TIL111	300540140
LS1	Buzzer (PB3120B01)	300950030
RL1	Reed Relay (RS5V)	300652030
PLA	Plug, Eurocard	352364010
SK1	Connector, 4 way	352304070
SK2	Connector, 26 way	352326100
SK?	Socket 40 way DIL	300584970
P1	Disconnect pin	355900550
P2	Disconnect pin	355900550
S?	Keyswitch 3 position (On front panel)	379618401
TP1 to TP15	Test Hooks	355400760

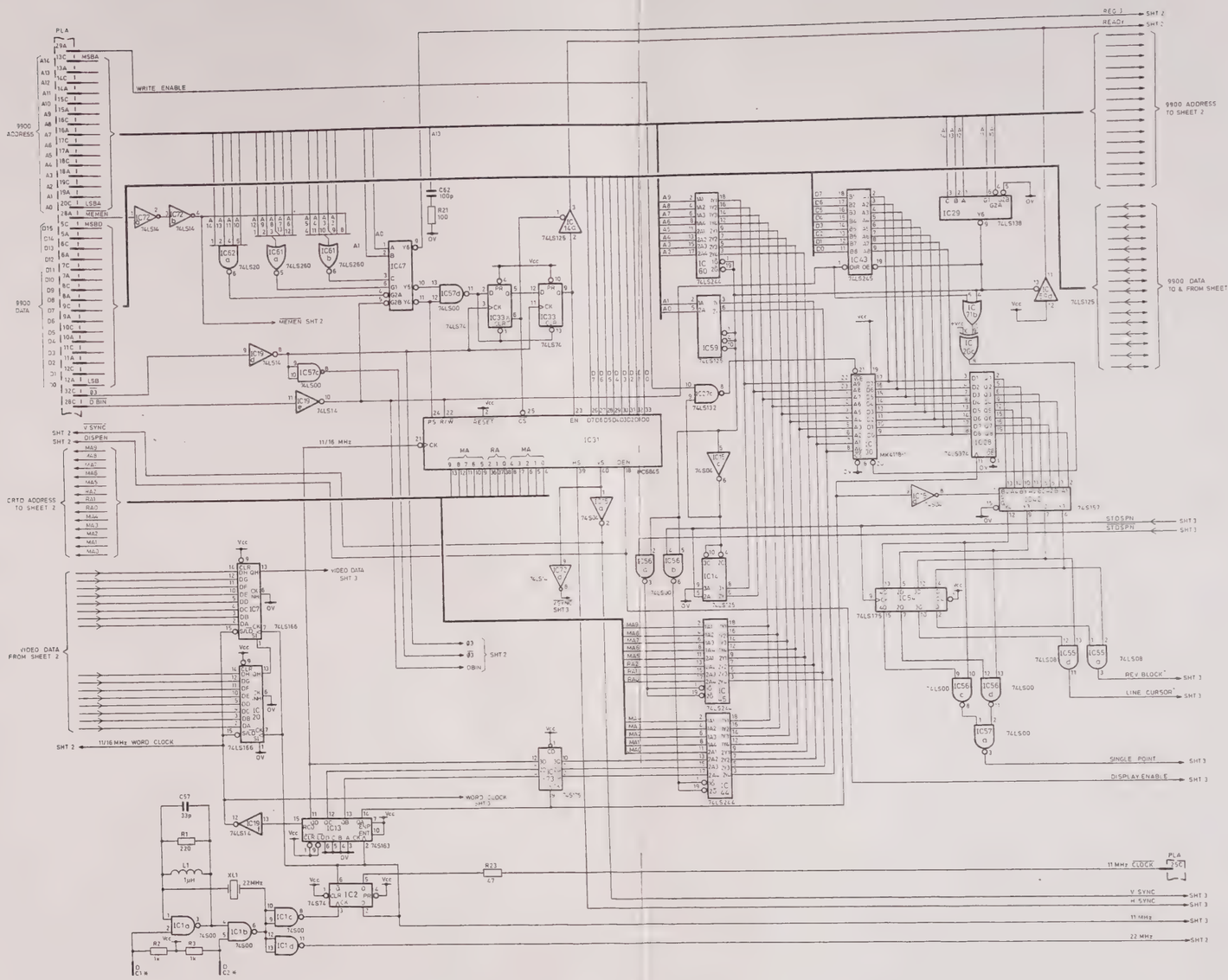


SYSTEM CONTROLLER (1)
12007501 Issue G Sheet 1

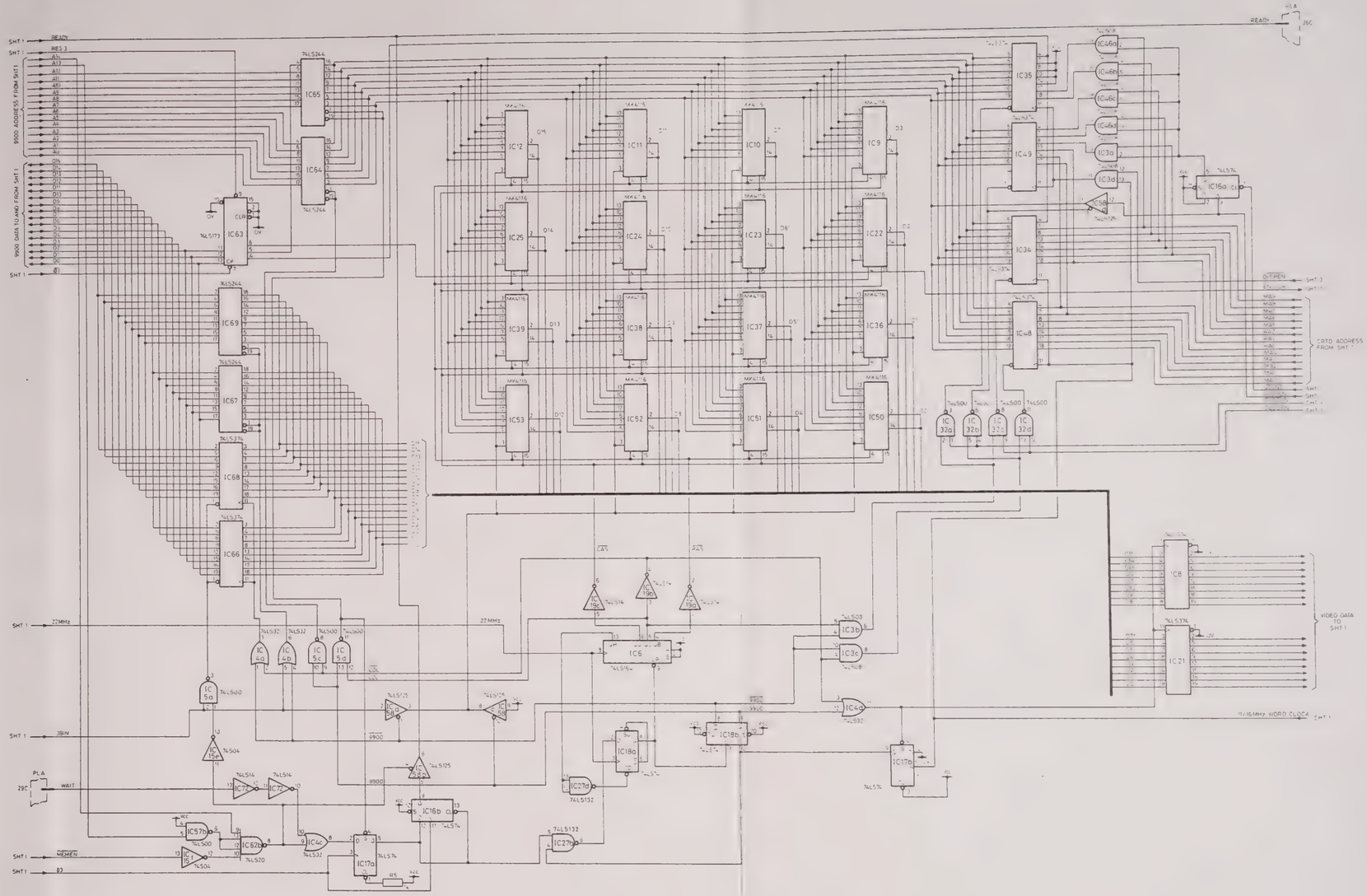


EPROM	PIN 18	PIN 19	PIN 20	PIN 21
1-2716	$\overline{OE}$	A10	$\overline{OE}$	Vpp
TMS 2516	PD/PE*	A10	$\overline{CS}$	Vpp
TMS 2532	A11	A10	PD/PGM*	Vpp

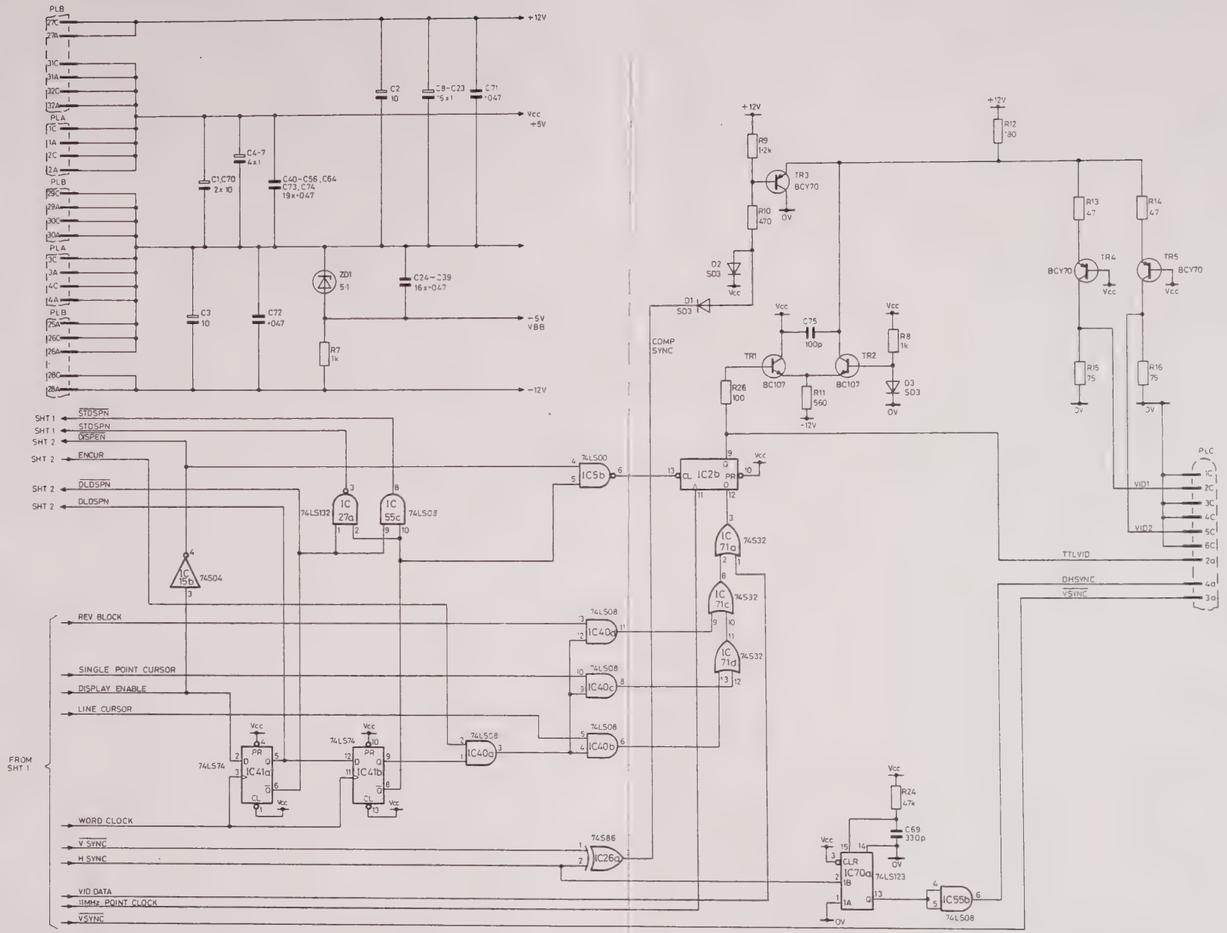

POWER SUPPLIES : IC65: PIN1 = Vcc PIN 8 = -5V
IC66: PIN16 = Vcc PIN 8 = GND
IC11
IC61
IC51
IC50
74LS374
74LS244
UPD0
UPD1
UPD2
UPD3
UPD4
UPD5
UPD6
UPD7
UPD8
UPD9
UPD10
UPD11
UPD12
UPD13
UPD14
UPD15
R/W
1200 IN EN
1200 OUT EN
P16
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
IC64
IC5
9902
UPA10
UPA11
UPA12
UPA13
UPA14
CRU OUT
CRU CLK
RS-432-EN SHT 1
FP EN SHT 1
IC67
74LS04
IC65
AM26LS30
IC66
AM26LS32
C26 47p
C27 47p
C29 47p
R17 470
R16 2-2k
IC66 PIN 14 (ENABLE)
IC65 PIN 4 (MODE)
IC66 PIN 12 (ENABLE)
IC65 PIN 5
Vcc
GND
PLC
RS-423 TxD DATA
RS-423 RxD DATA
RS-423 RTS
RS-423 CTS
RS-423 DSR
RS-423 GND
RS-423 SIG GND
RS-423 DTR
FP RxD DATA
FP TxD DATA
FP DCD
FP DSR
FP RTS
FP CTS
FP SIG GND
FP GND
FP INT SHT 2
RS-423 INT SHT 2
CRU IN SHT 1



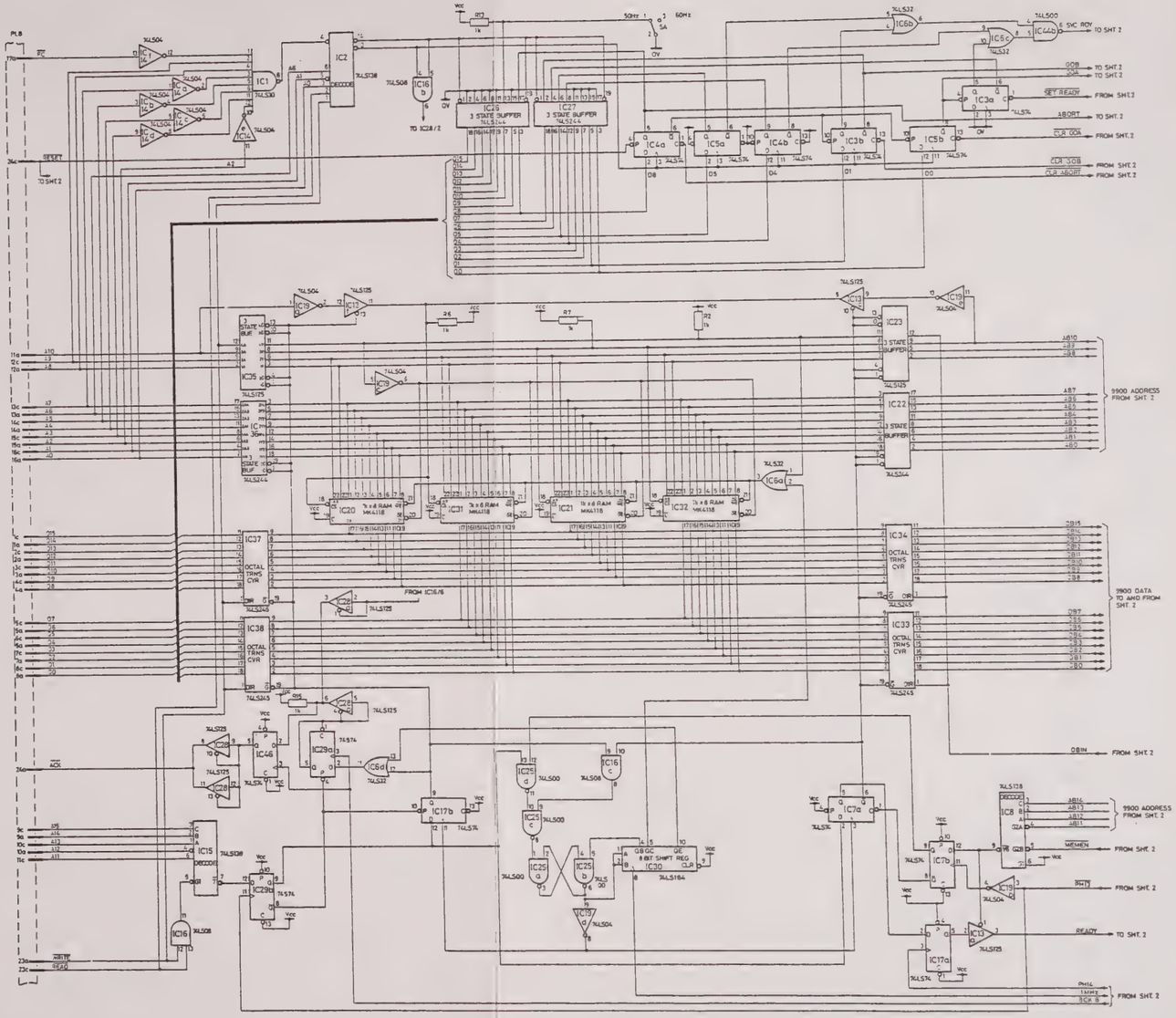
DISPLAY INTERFACE:
VIDEO STORE AND DRIVE (1)
12007502 Issue G Sheet 1



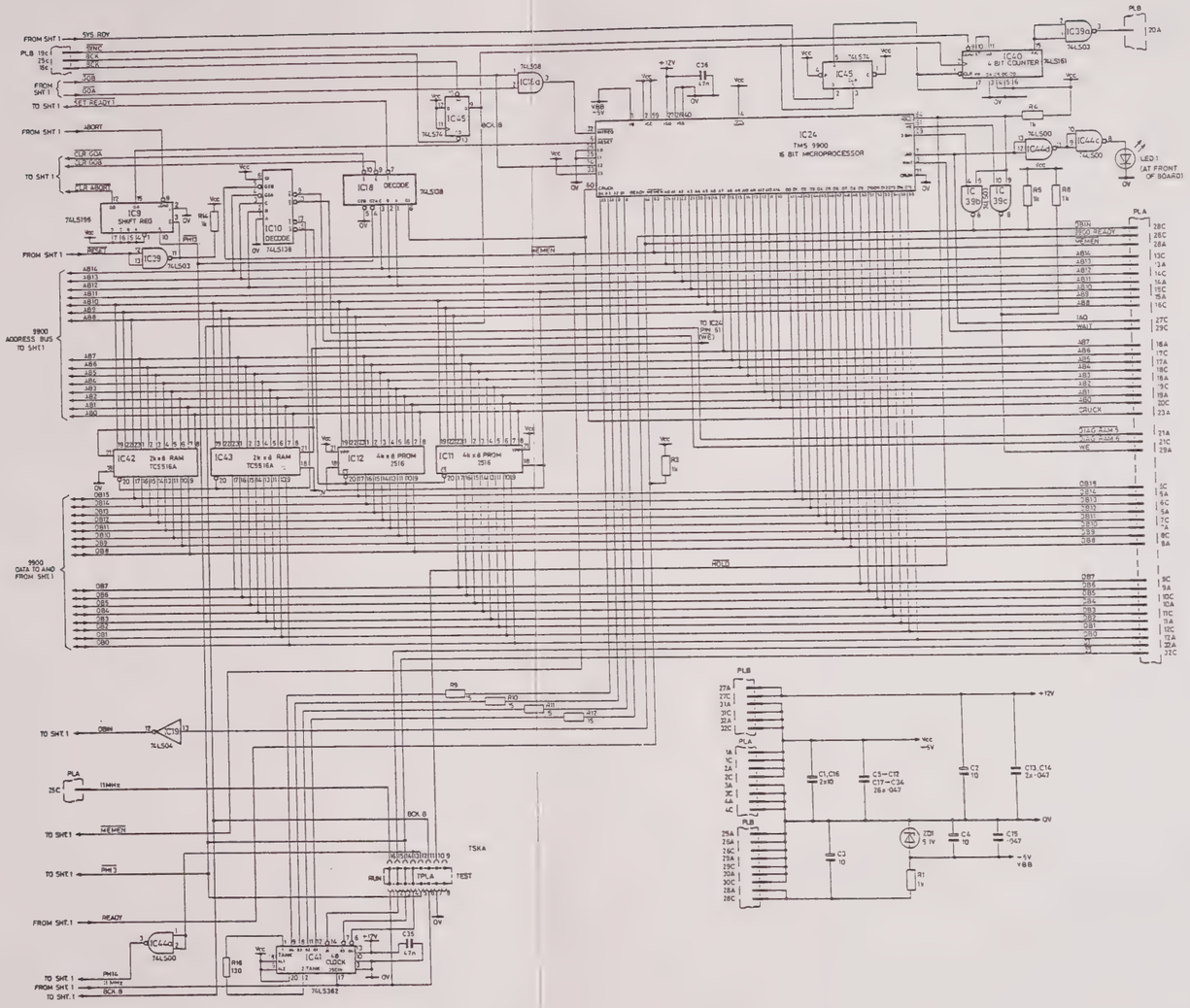
DISPLAY INTERFACE:
VIDEO STORE AND DRIVE (2)
12007502 Issue G Sheet 2



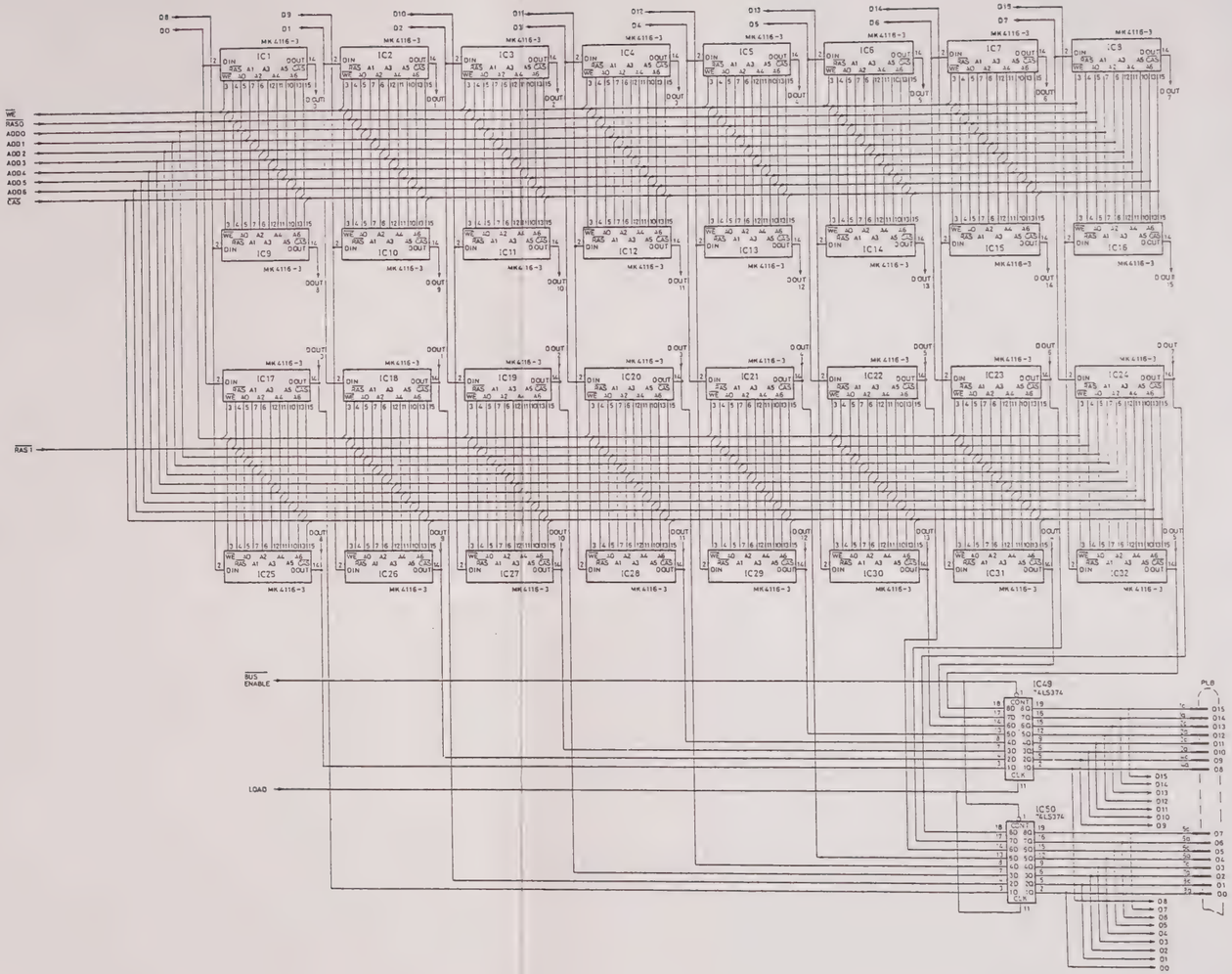
DISPLAY INTERFACE:
VIDEO STORE AND DRIVE (3)
12007502 Issue G Sheet 3



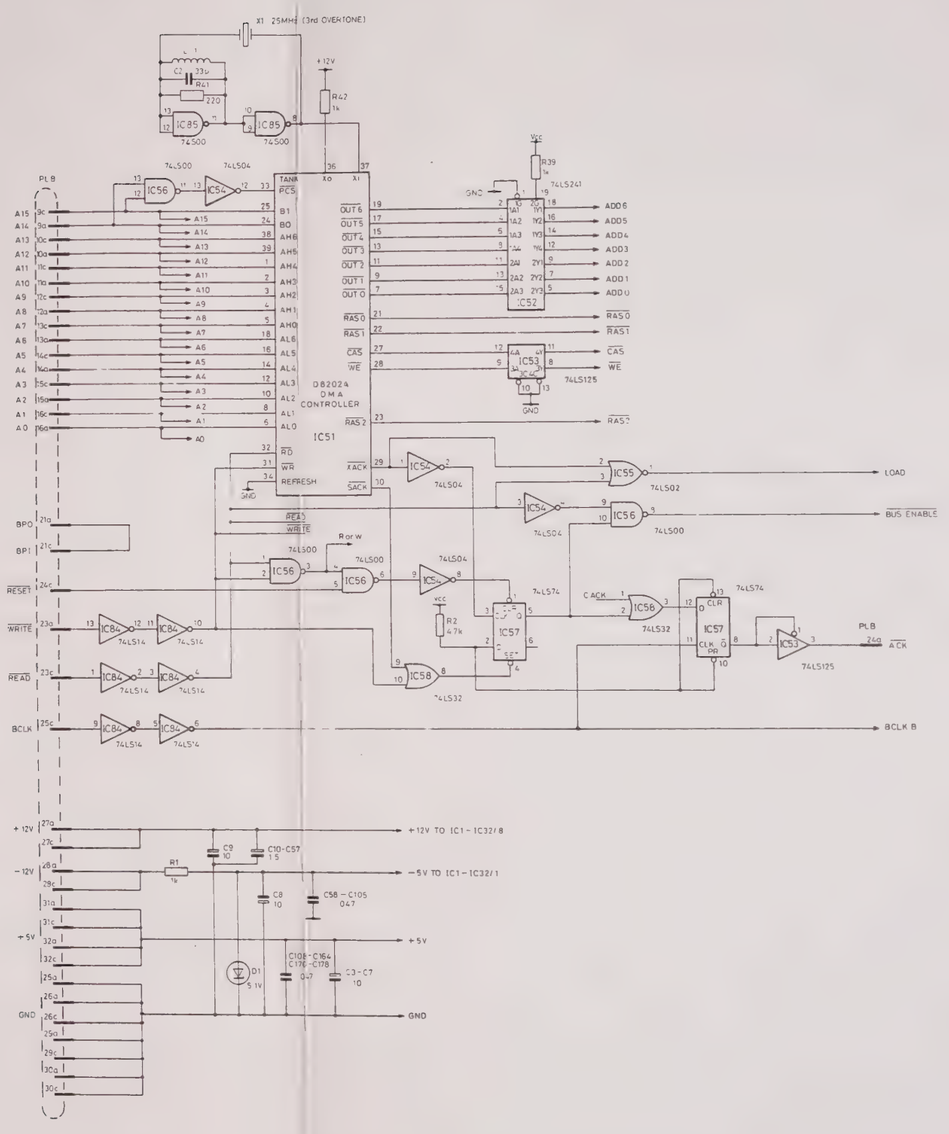
DISPLAY BUFFER AND CONTROL (1)
12007503 Issue J Sheet 1



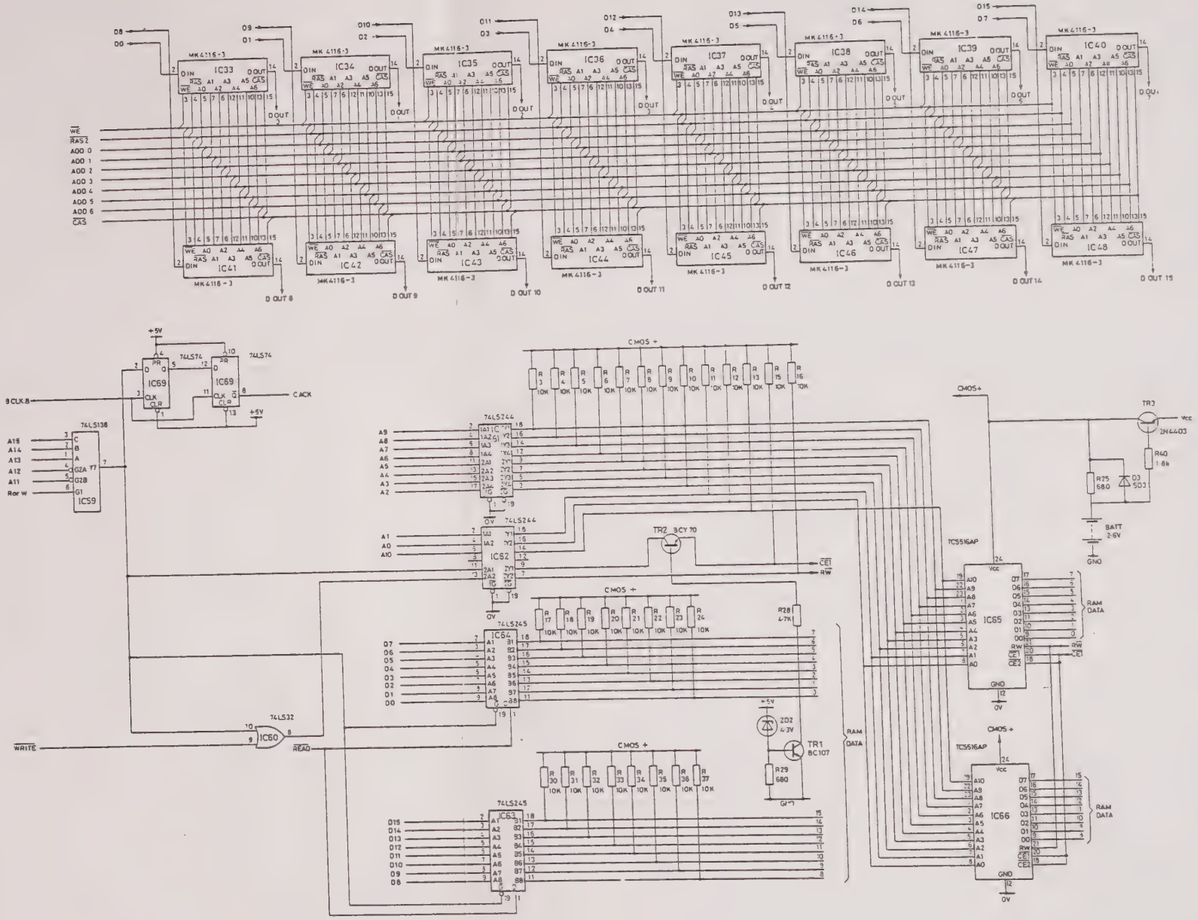
DISPLAY BUFFER AND CONTROL (2)
12007503 Issue J Sheet 2



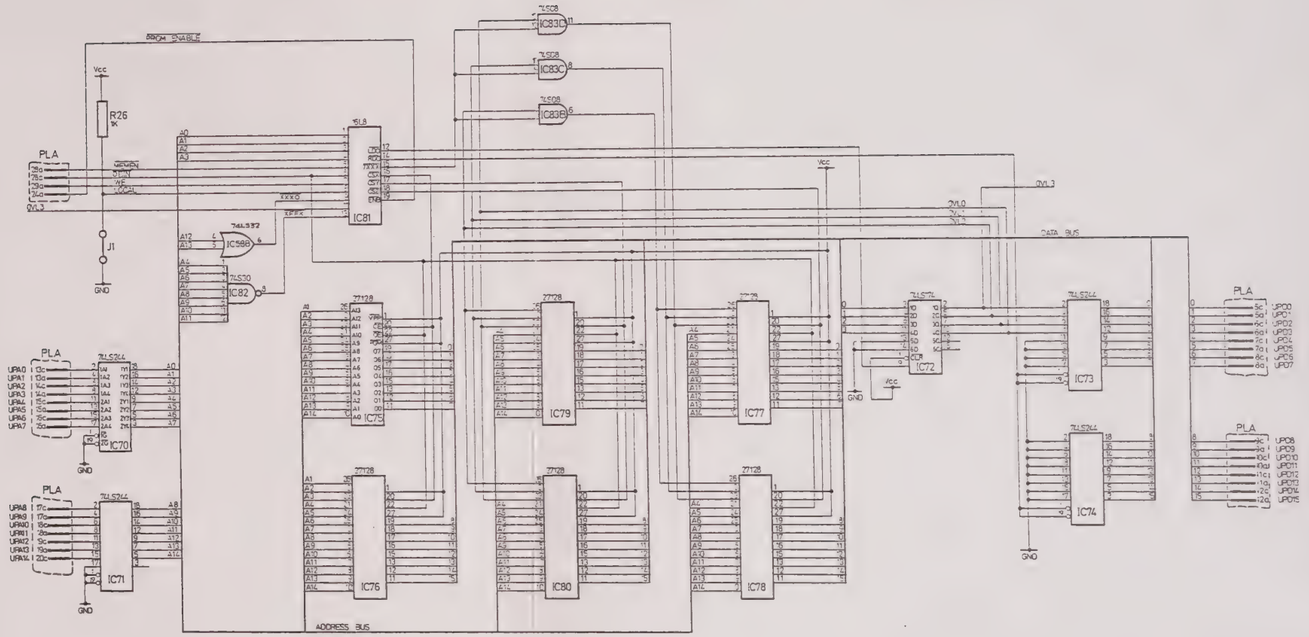
DATA STORE (1)
12007504 Issue J Sheet 1



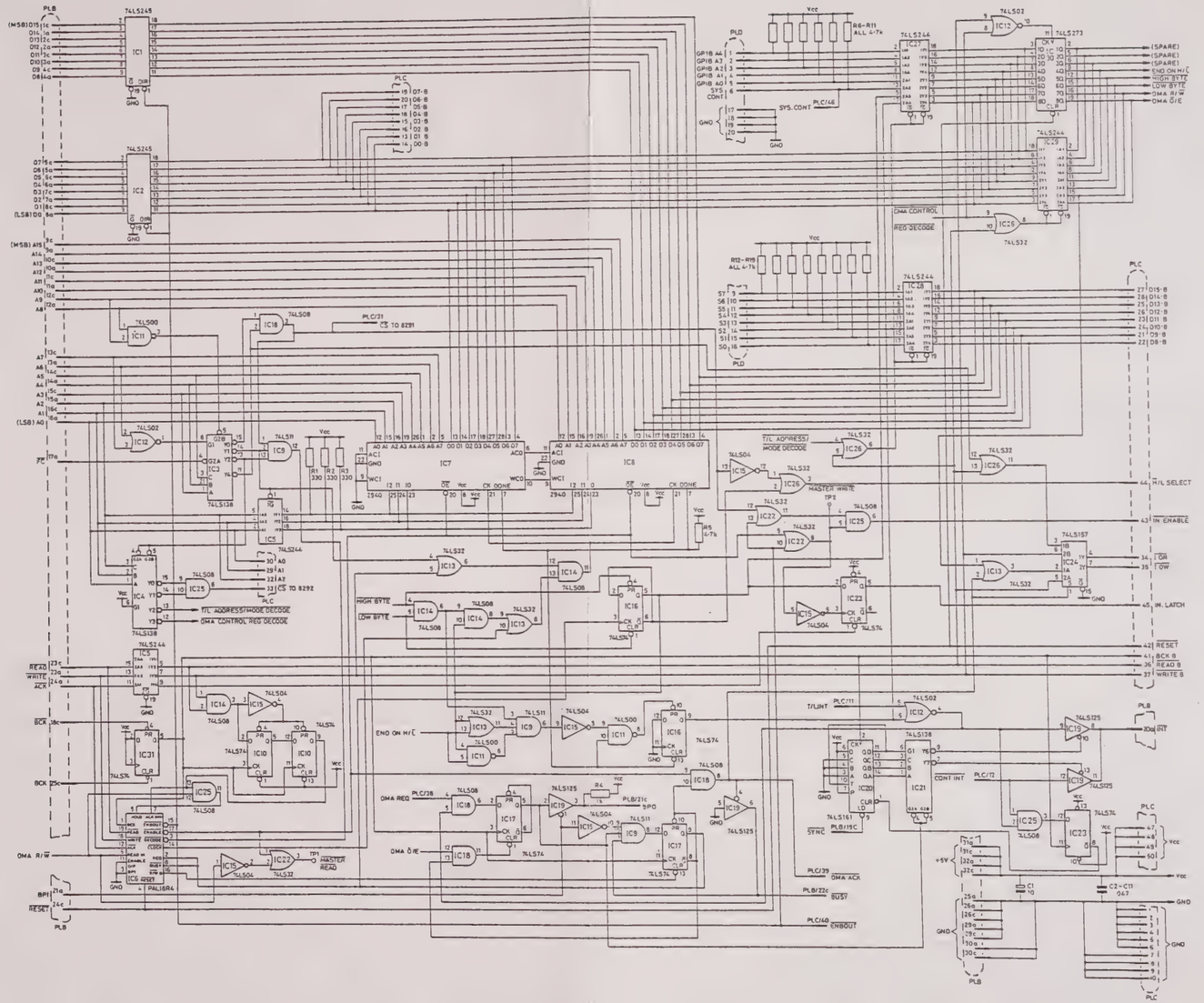
DATA STORE (2)
12007504 Issue H Sheet 2



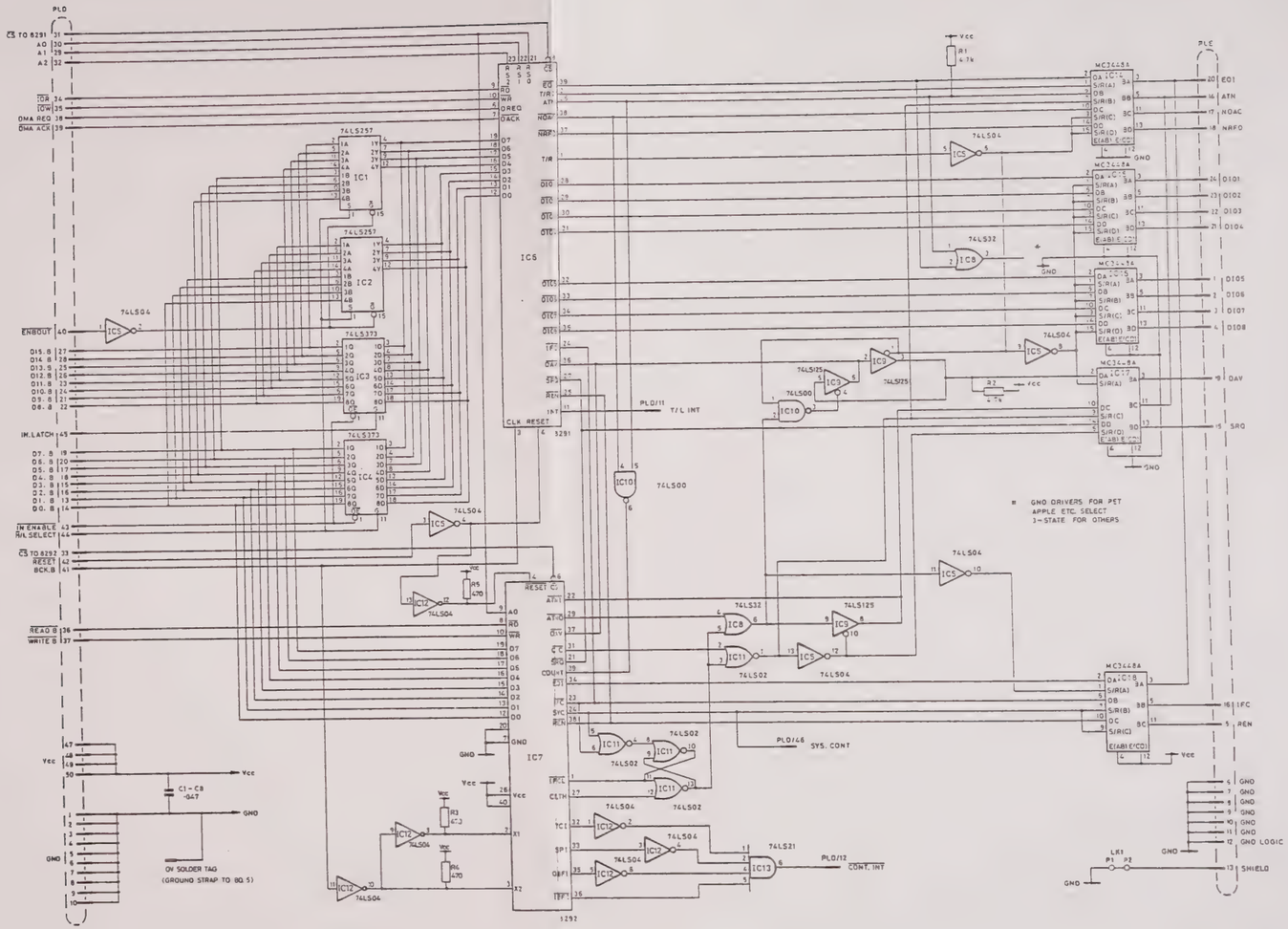
DATA STORE (3)
12007504 Issue J Sheet 3



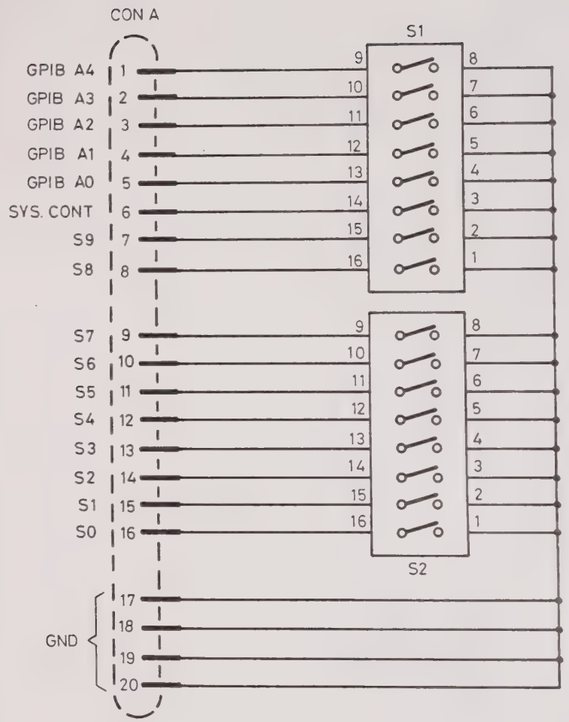
DATA STORE (4)
12007504 Issue J Sheet 4



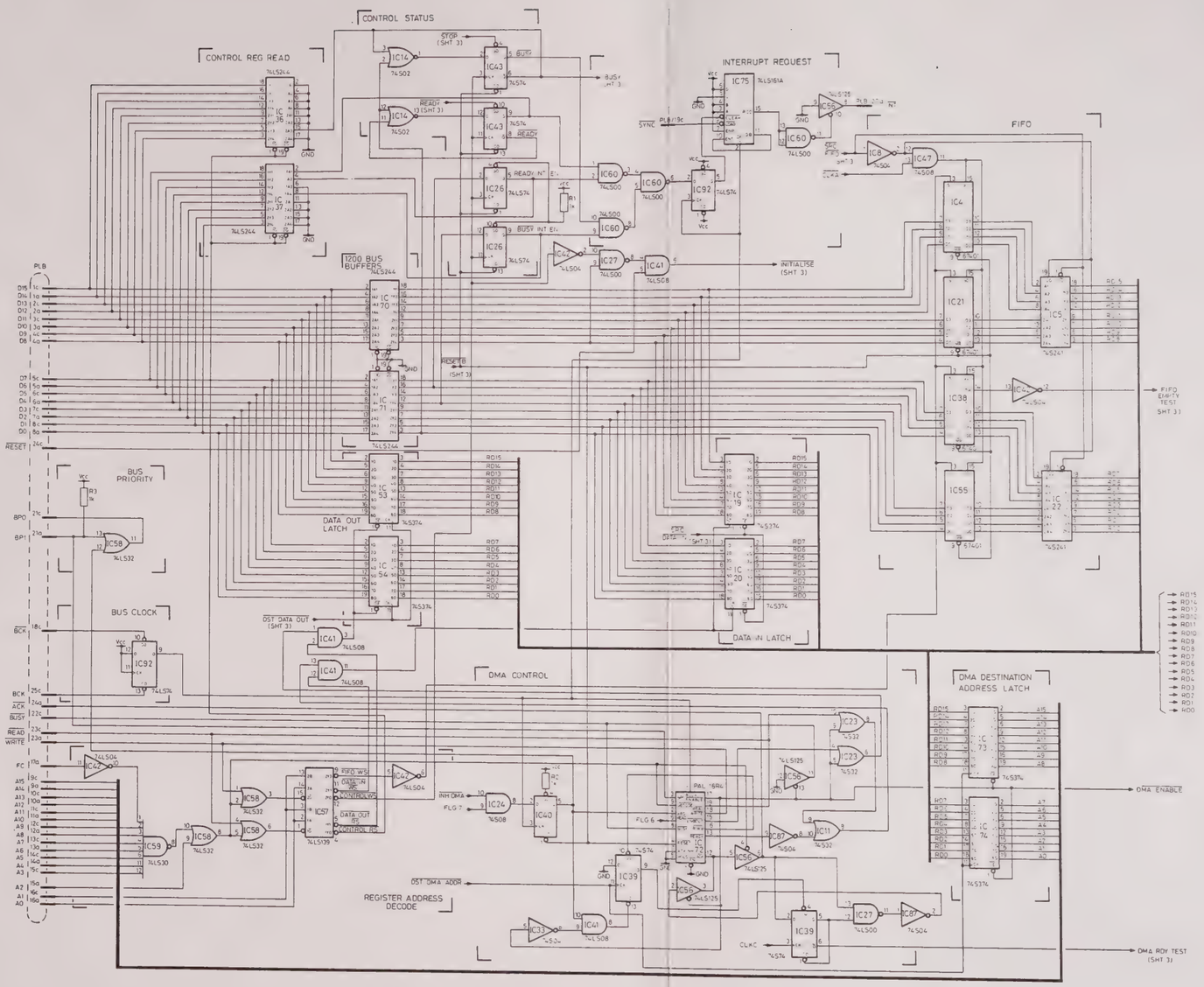
GPIB CONTROL LOGIC
12007505 Issue F Sheet 1



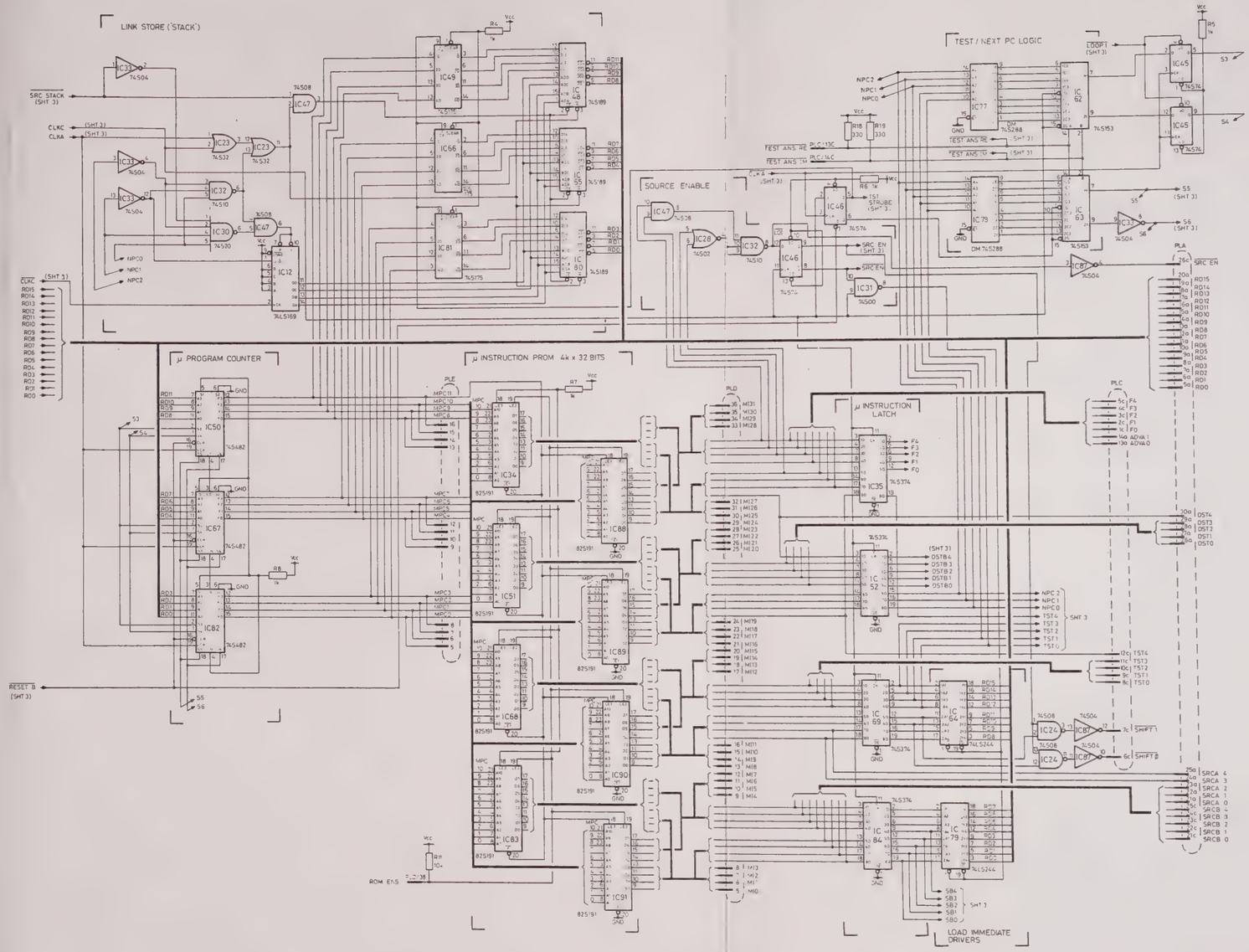
GPIB INTERFACE
12007506 Issue E Sheet 1



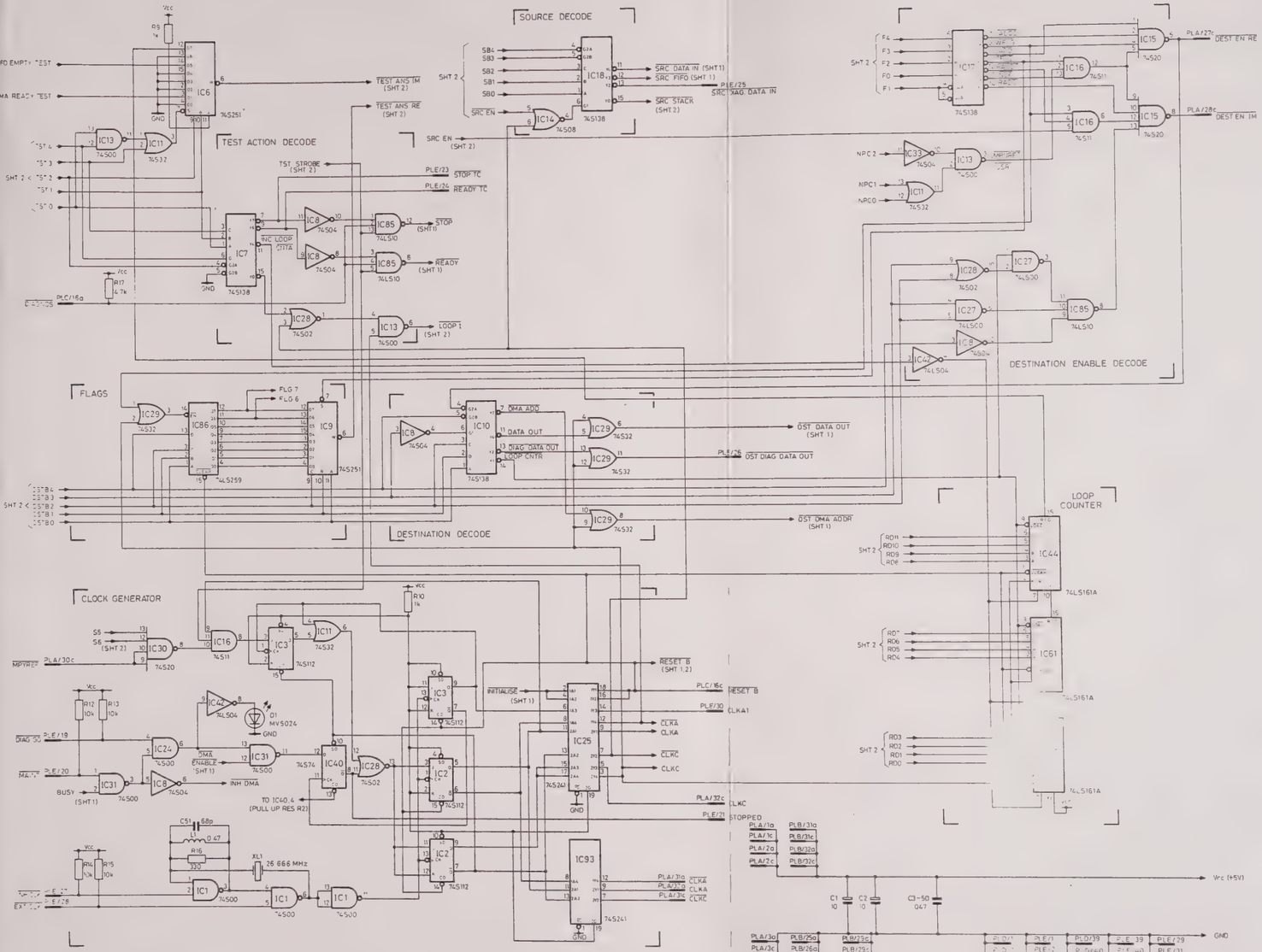
GPIB ADDRESS AND FUNCTION SWITCHES
12007507 Issue B Sheet 1



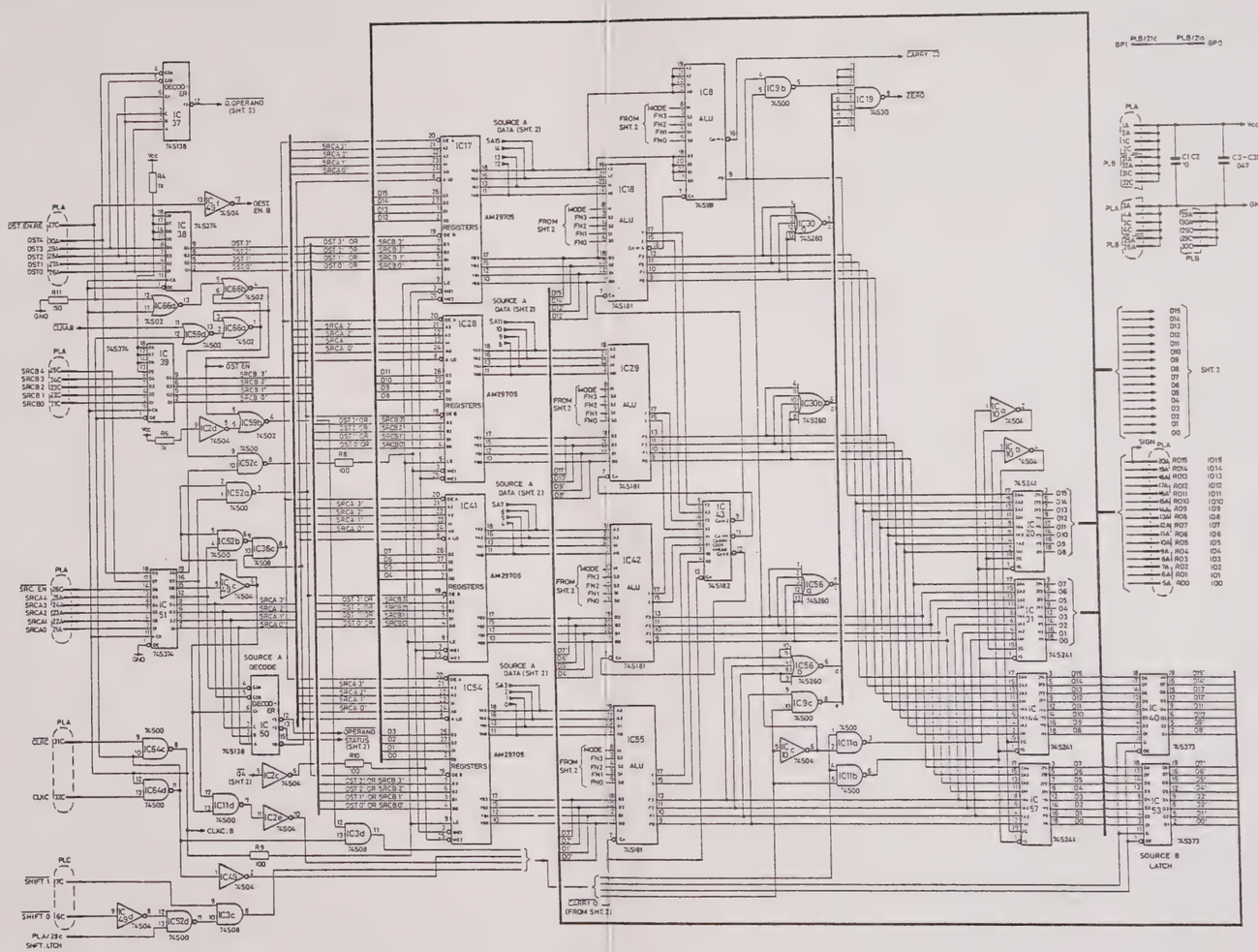
ARRAY PROCESSOR CONTROL (1)
12007508 Issue C Sheet 1



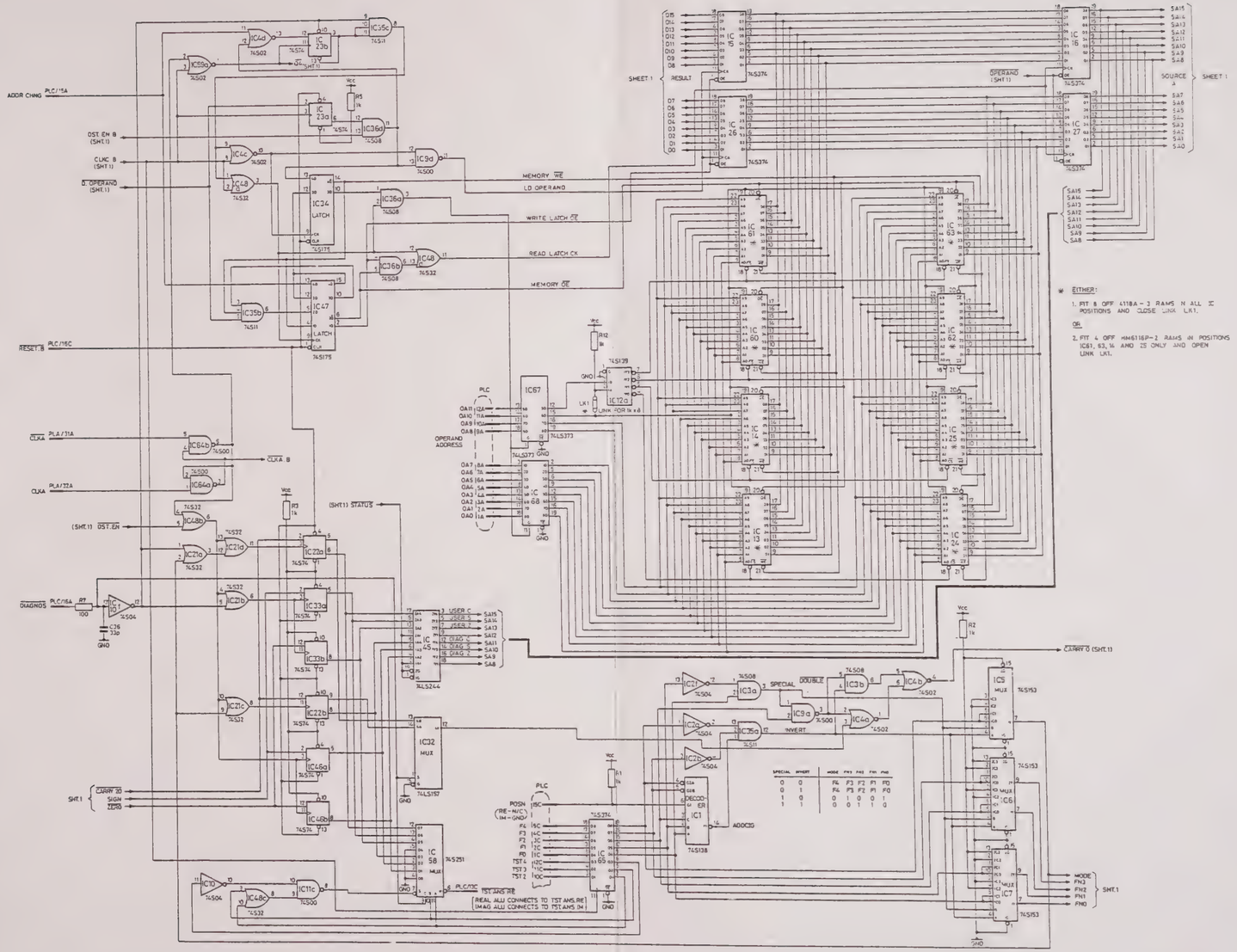
ARRAY PROCESSOR CONTROL (2)
12007508 Issue C Sheet 2



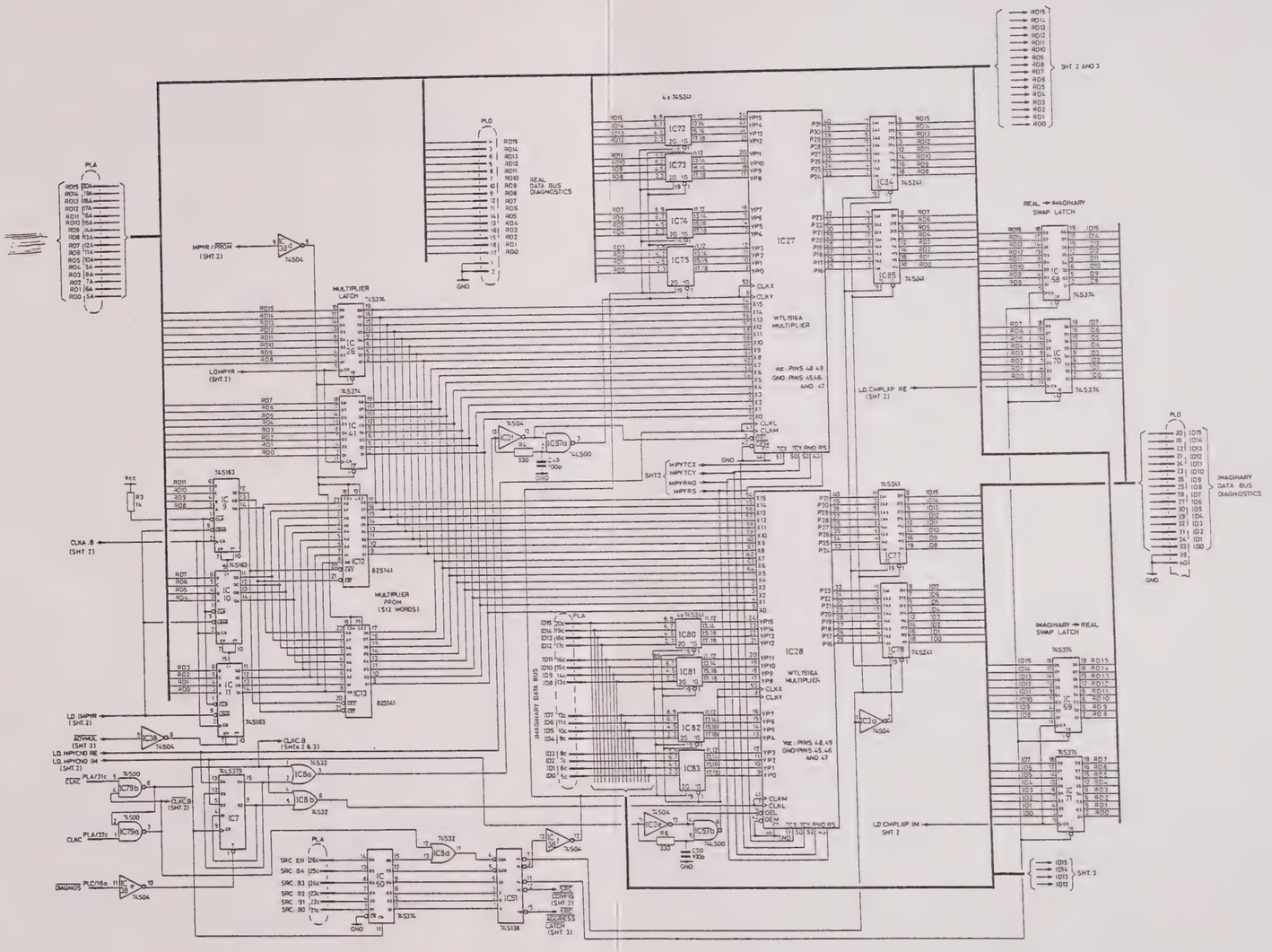
ARRAY PROCESSOR CONTROL (3)
12007508 Issue C Sheet 3



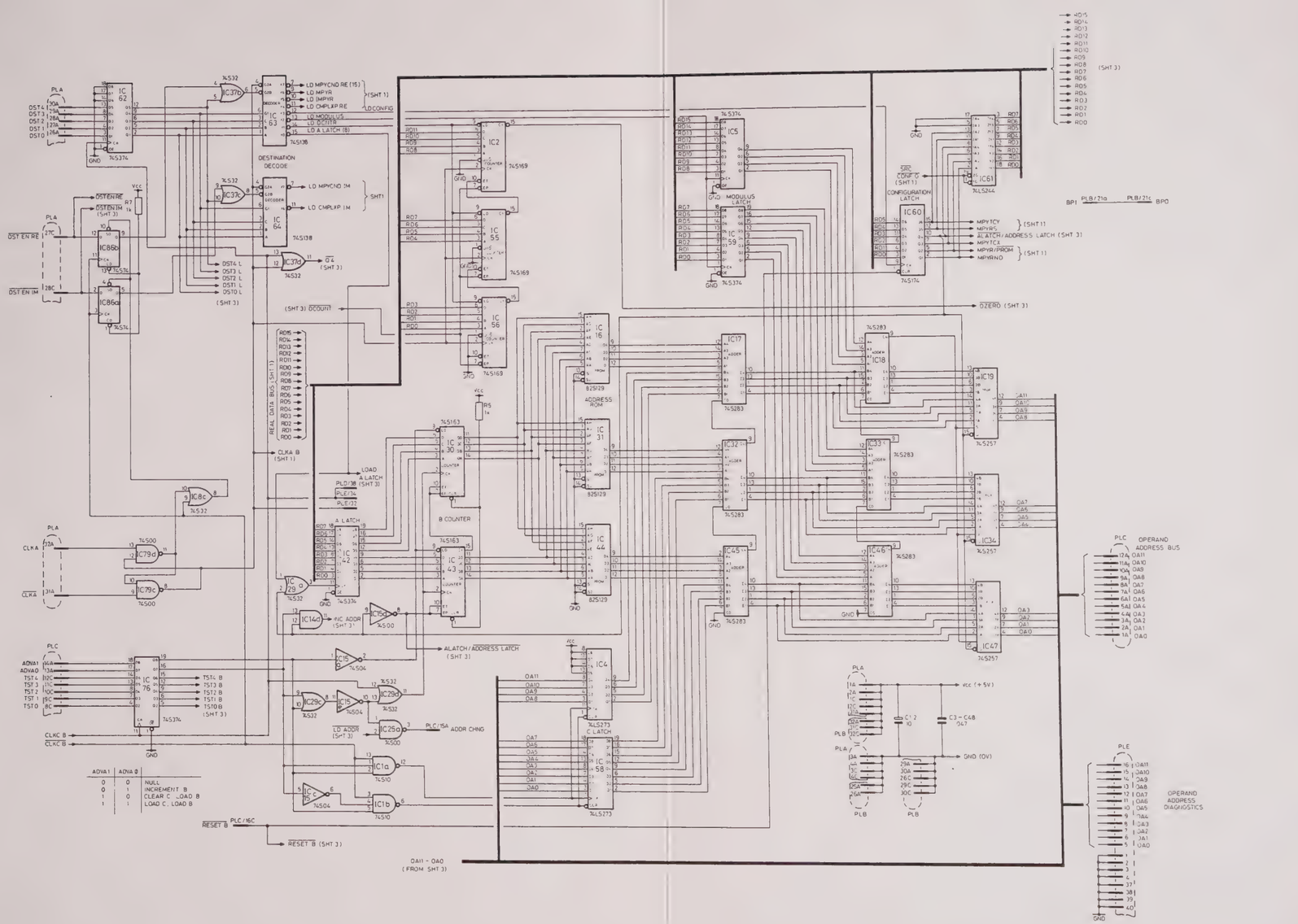
ARRAY PROCESSOR ALU (1)
12007509 Issue G Sheet 1



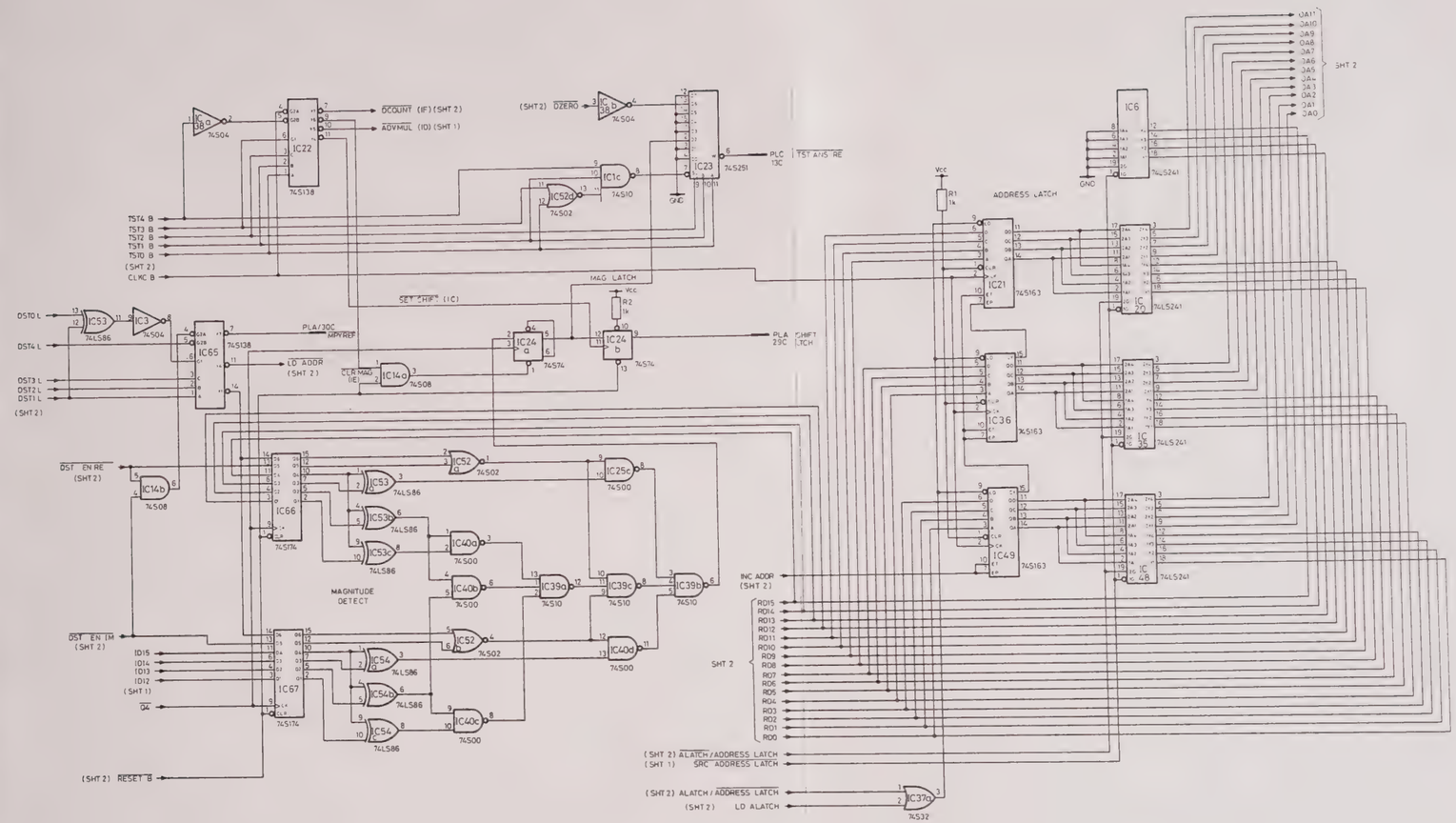
ARRAY PROCESSOR ALU (2)
12007509 Issue G Sheet 2



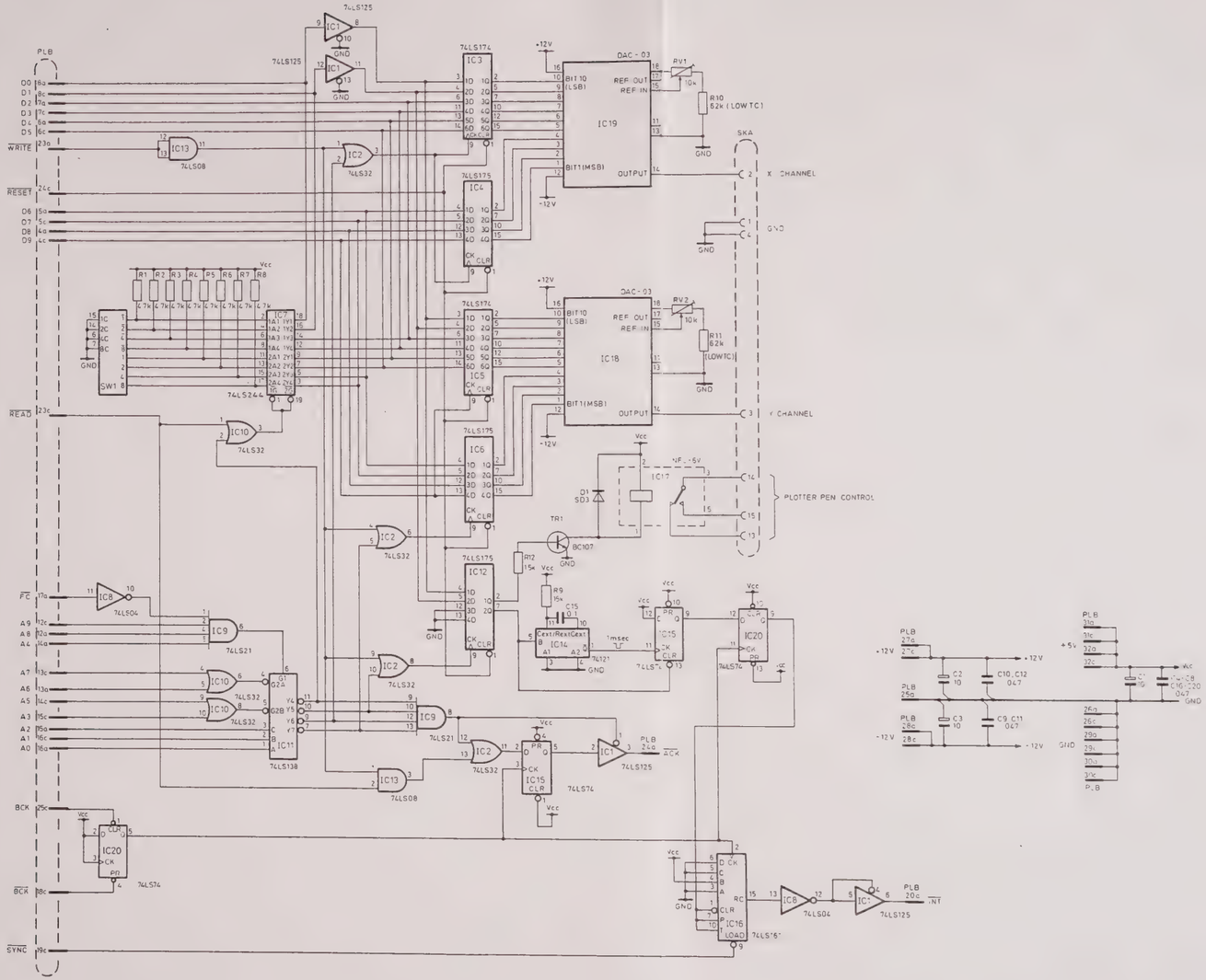
ARRAY PROCESSOR MULTIPLIER (1)
12007510 Issue F Sheet 1



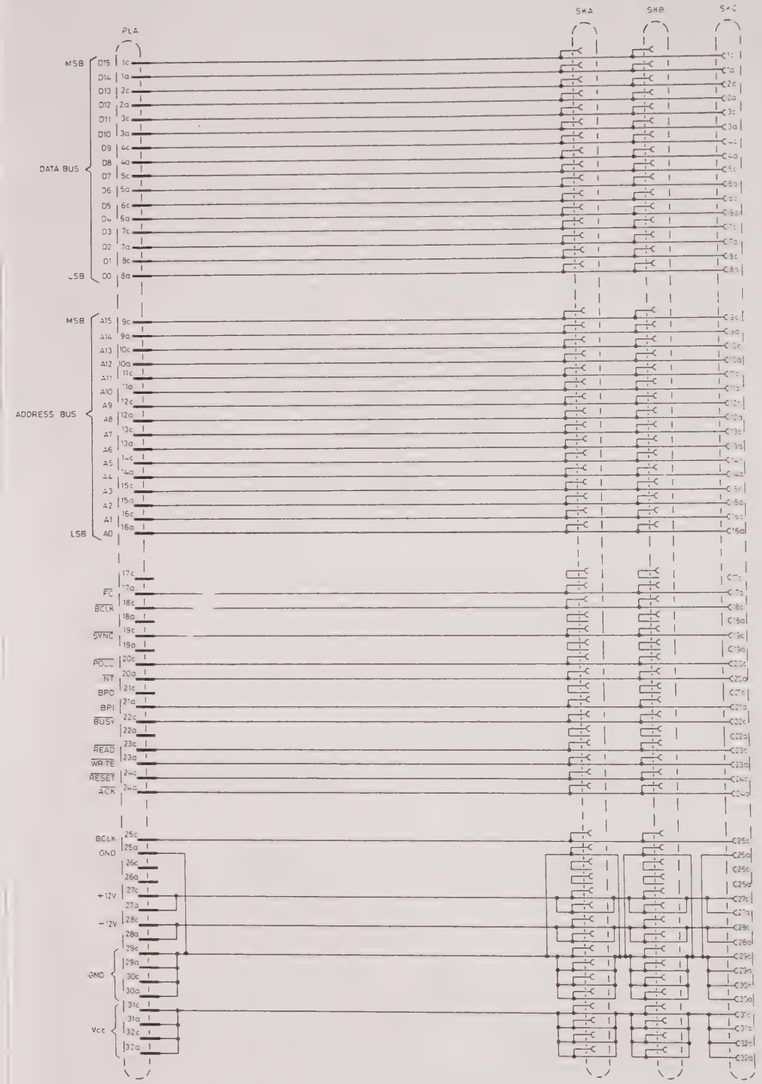
ARRAY PROCESSOR MULTIPLIER (2)
12007510 Issue E Sheet 2



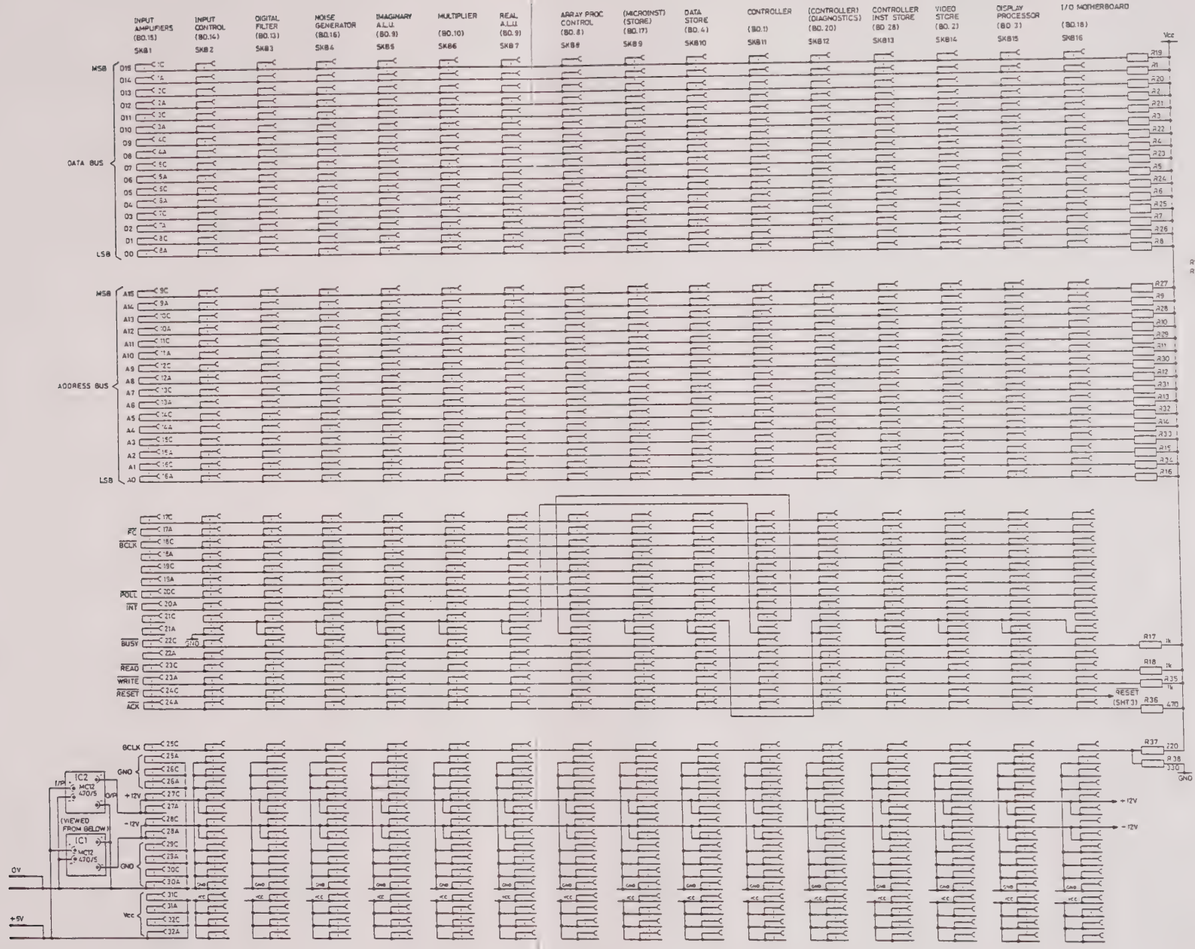
ARRAY PROCESSOR MULTIPLIER (3)
12007510 Issue E Sheet 3



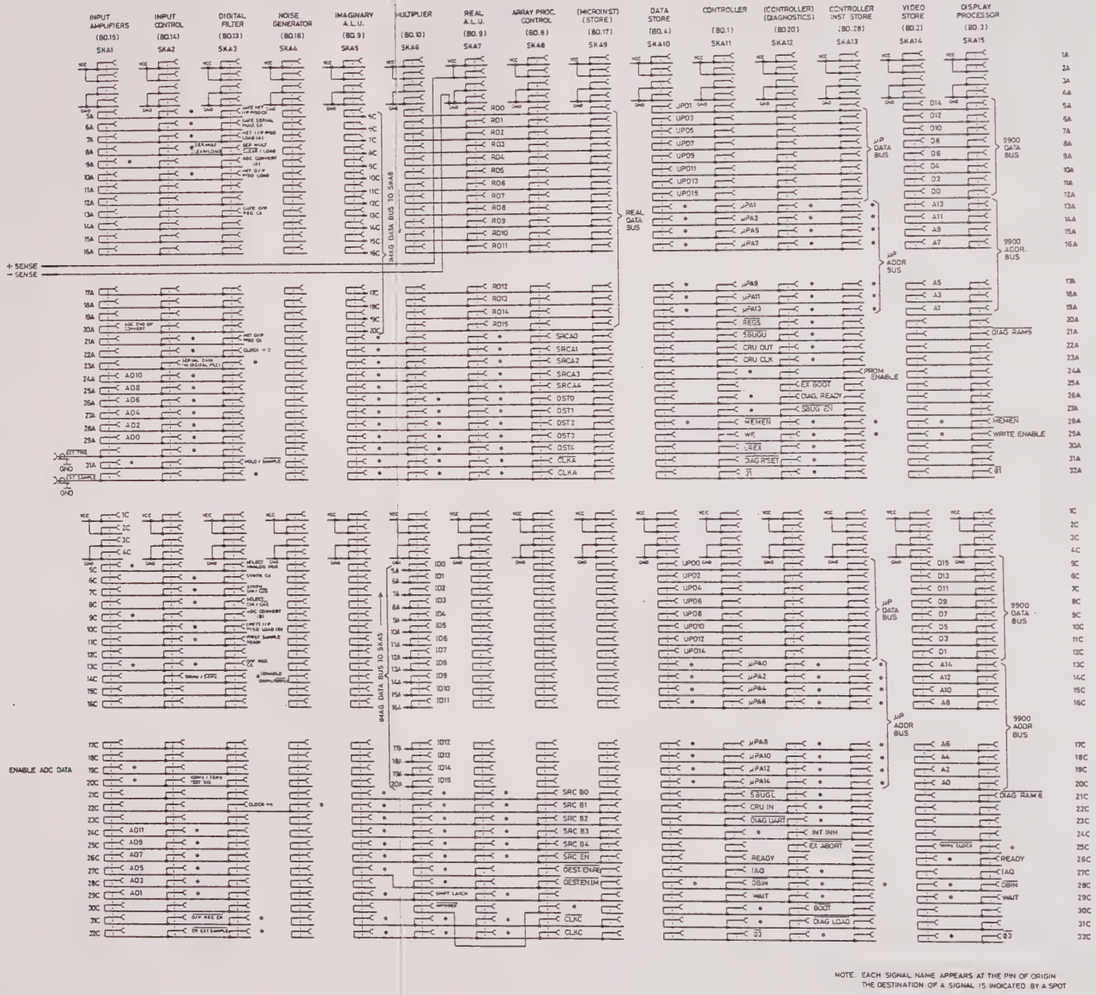
X, Y PLOTTER
12007511 Issue E Sheet 1



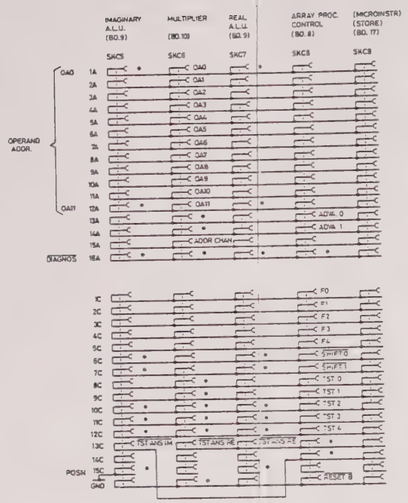
I/O DAUGHTER BOARD
12007518 Issue G Sheet 1

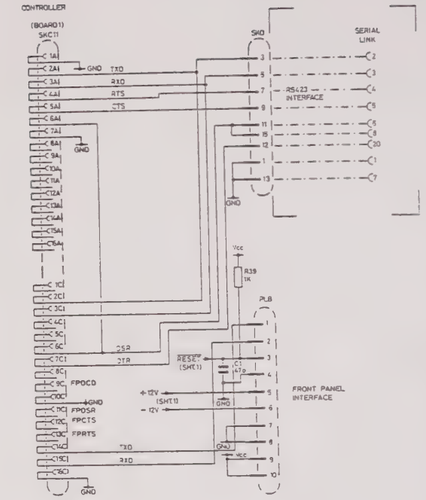


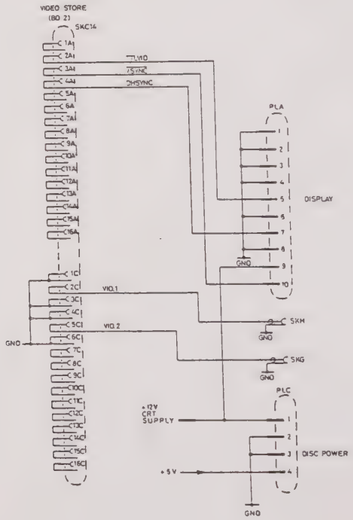
RVC MOTHER BOARD (1)
12007S19 Issue K Sheet 1



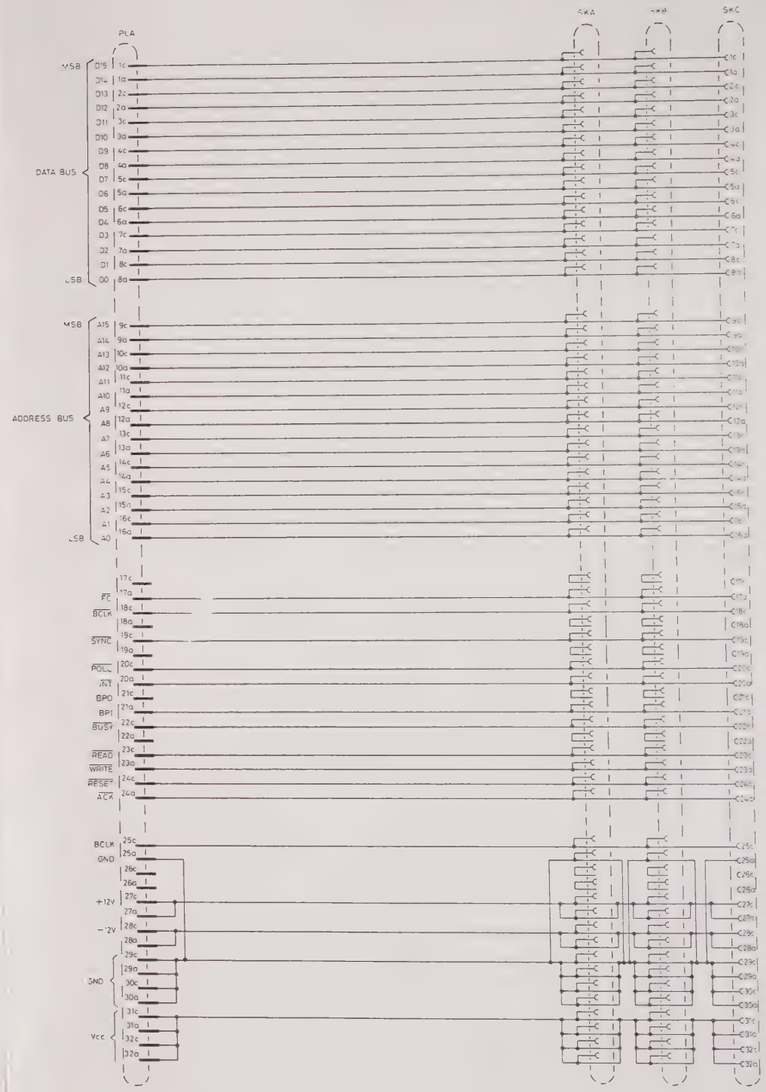
NOTE: EACH SIGNAL NAME APPEARS AT THE PIN OF ORIGIN
THE DESTINATION OF A SIGNAL IS INDICATED BY A SPOT



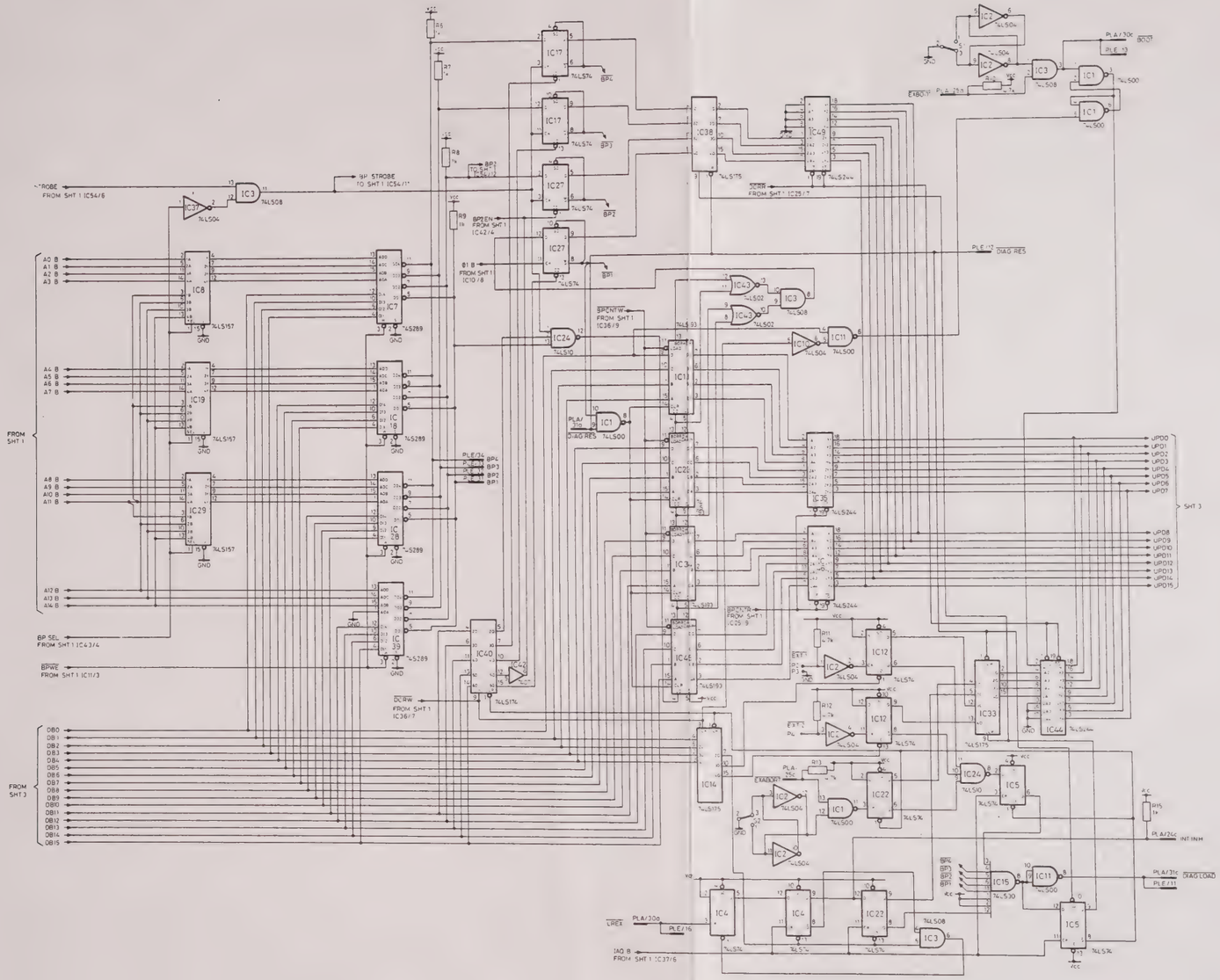




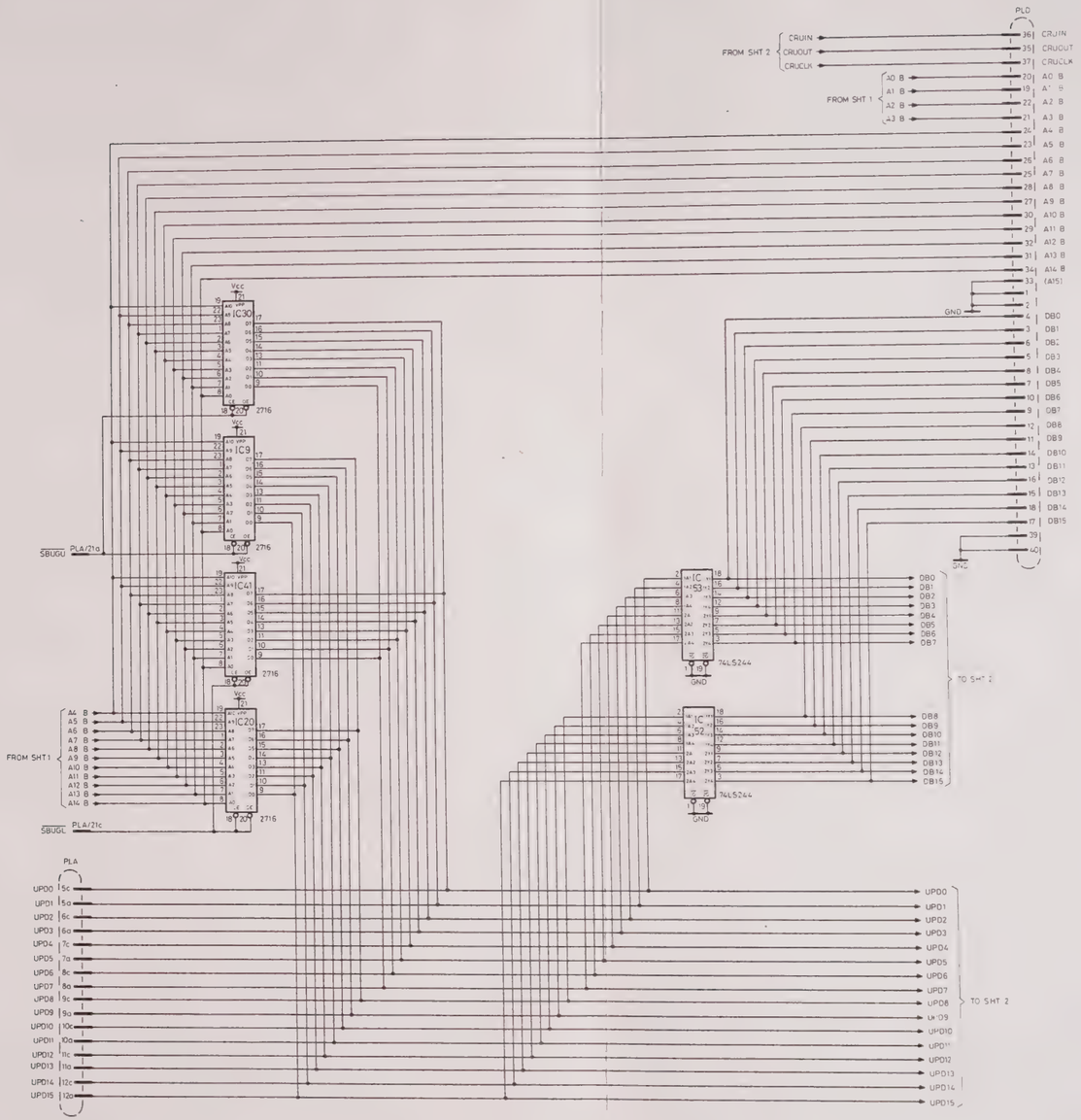
RVC MOTHER BOARD (3)
12007519 Issue K Sheet 3

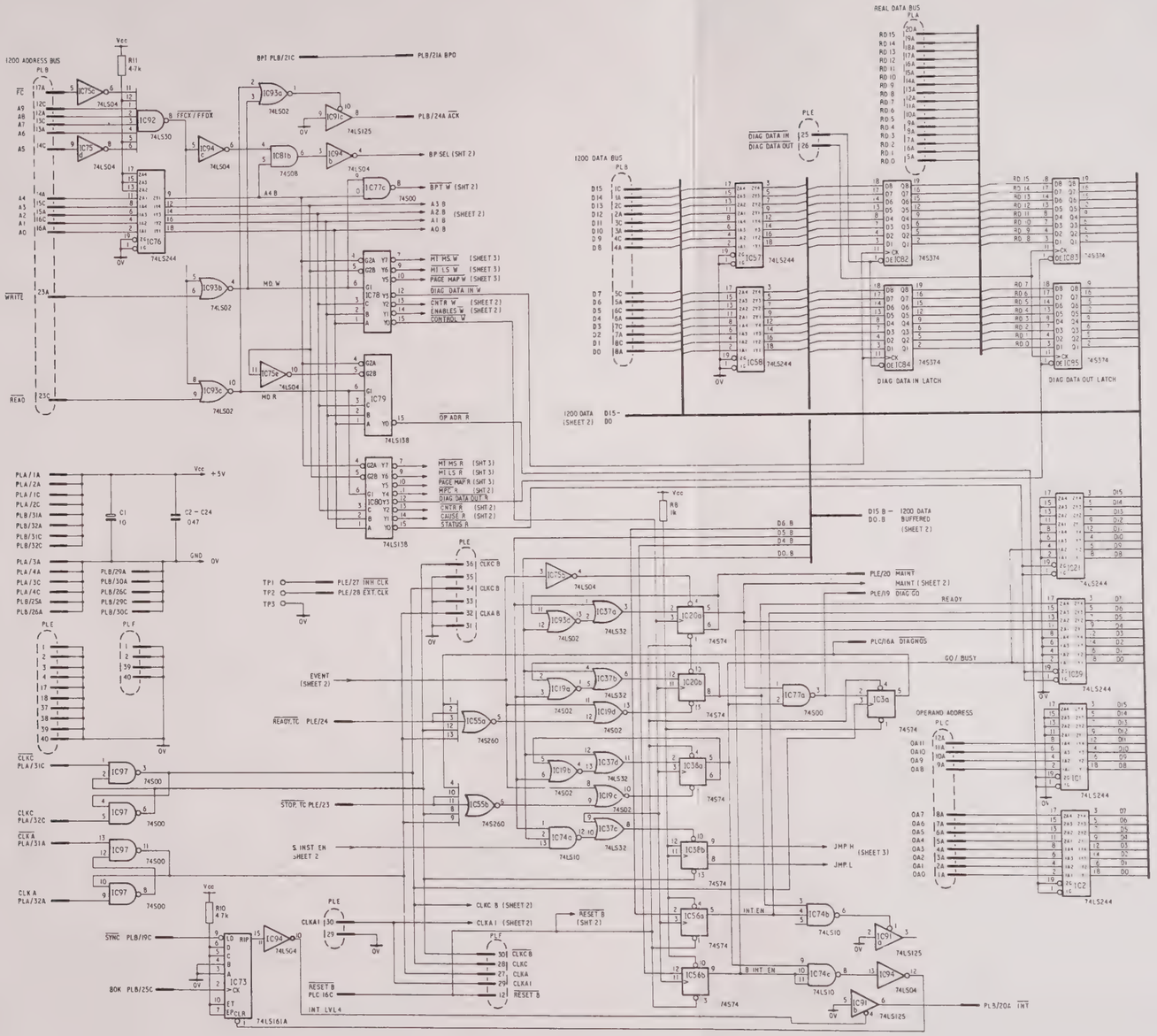


I/O DAUGHTER BOARD
12007518 Issue G Sheet 1

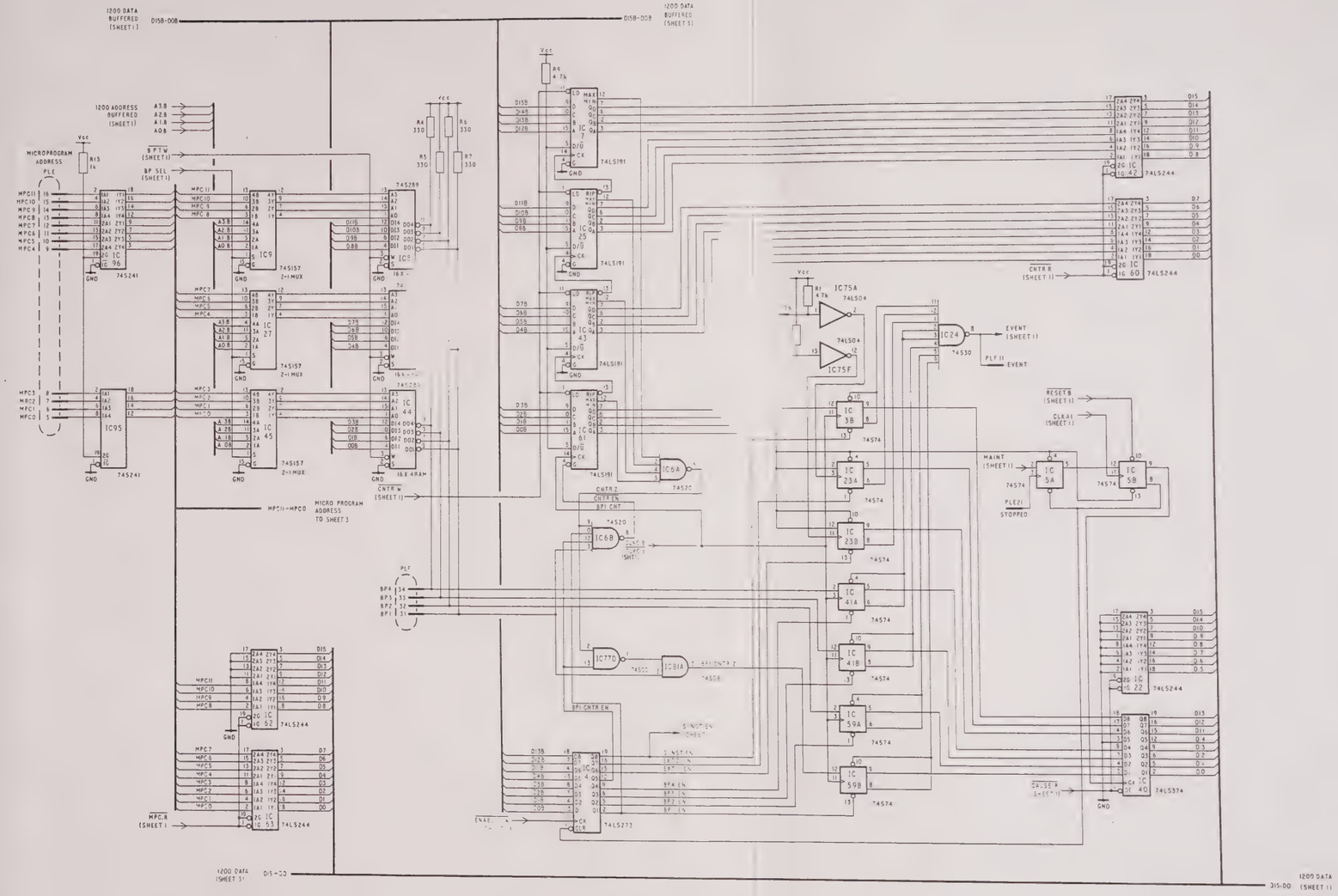


CONTROLLER DIAGNOSTIC (2)
12007520 Issue C Sheet 2

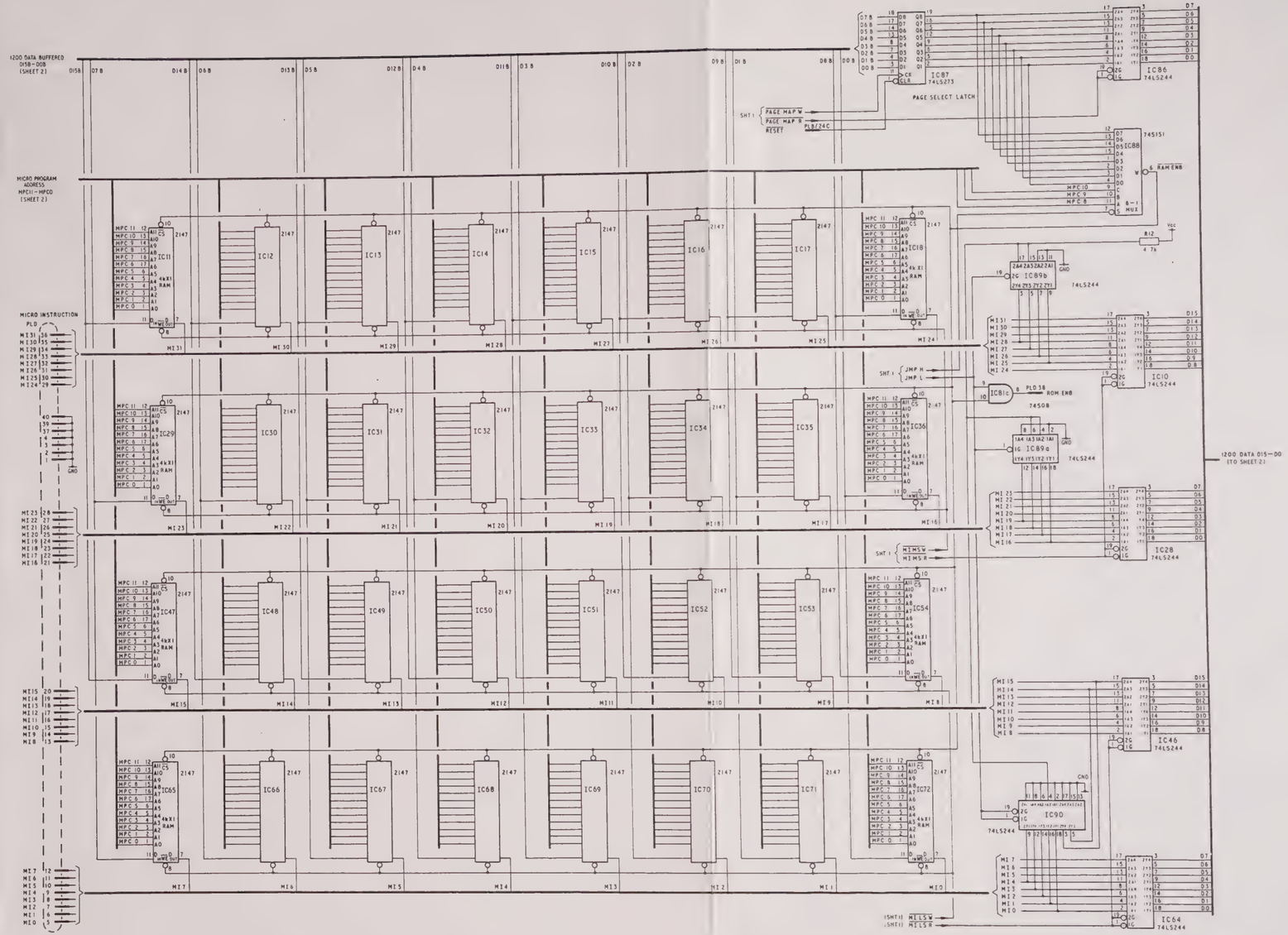

PLD
FROM SHT 2
CRUIN
CRUOUT
CRUCLK
FROM SHT 1
A0 B
A1 B
A2 B
A3 B
A4 B
A5 B
A6 B
A7 B
A8 B
A9 B
A10 B
A11 B
A12 B
A13 B
A14 B
(A15)
GND
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DB8
DB9
DB10
DB11
DB12
DB13
DB14
DB15
Vcc
IC30
IC9
IC41
IC20
2716
SBUGU
PLA/21o
SBUGL
PLA/21c
IC 53
IC 52
74LS244
TO SHT 2
PLA
UPD0
UPD1
UPD2
UPD3
UPD4
UPD5
UPD6
UPD7
UPD8
UPD9
UPD10
UPD11
UPD12
UPD13
UPD14
UPD15



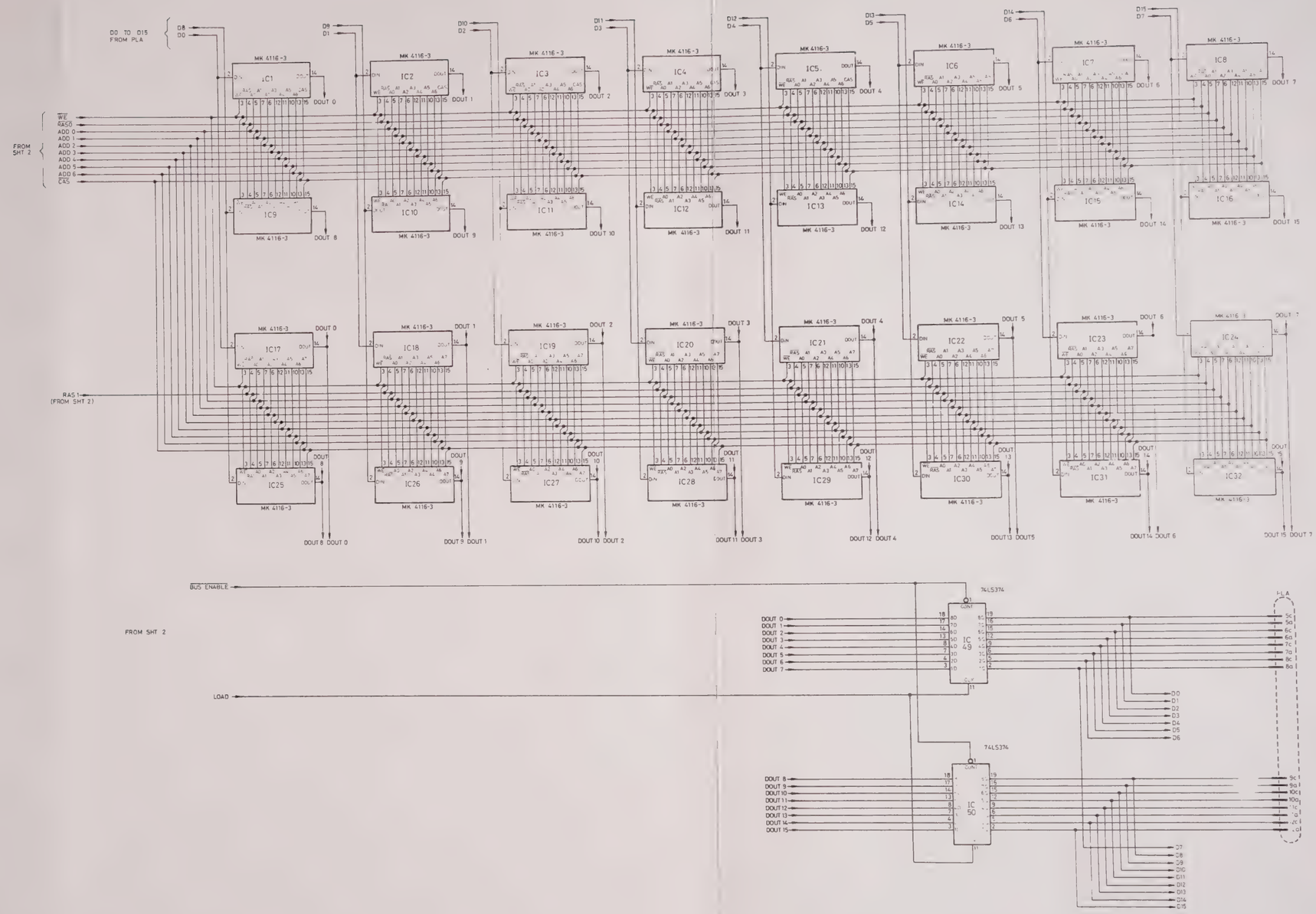
ARRAY PROCESSOR DIAGNOSTIC (1)
12007523 Issue C Sheet 1



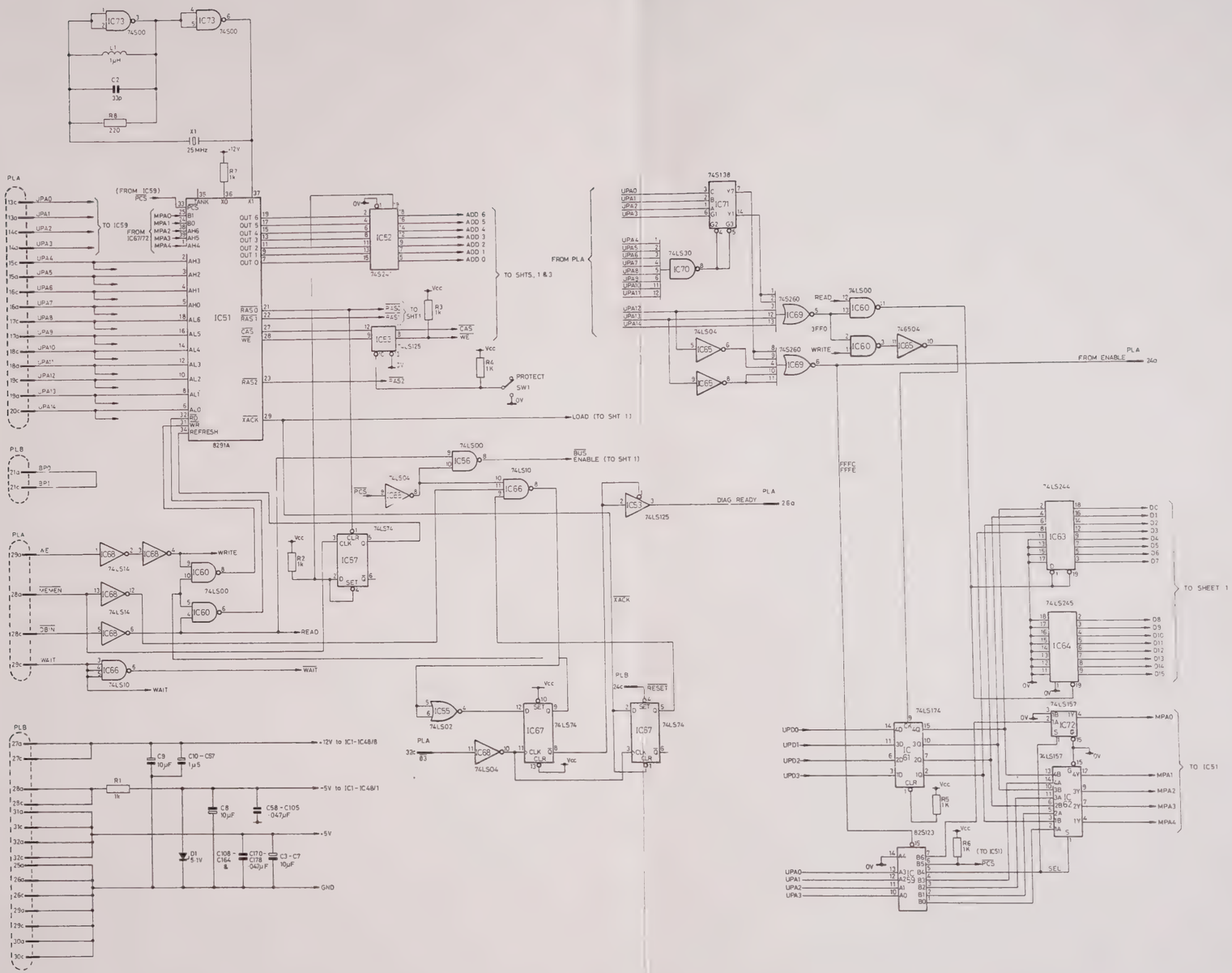
ARRAY PROCESSOR DIAGNOSTIC (2)
12007523 Issue C Sheet 2



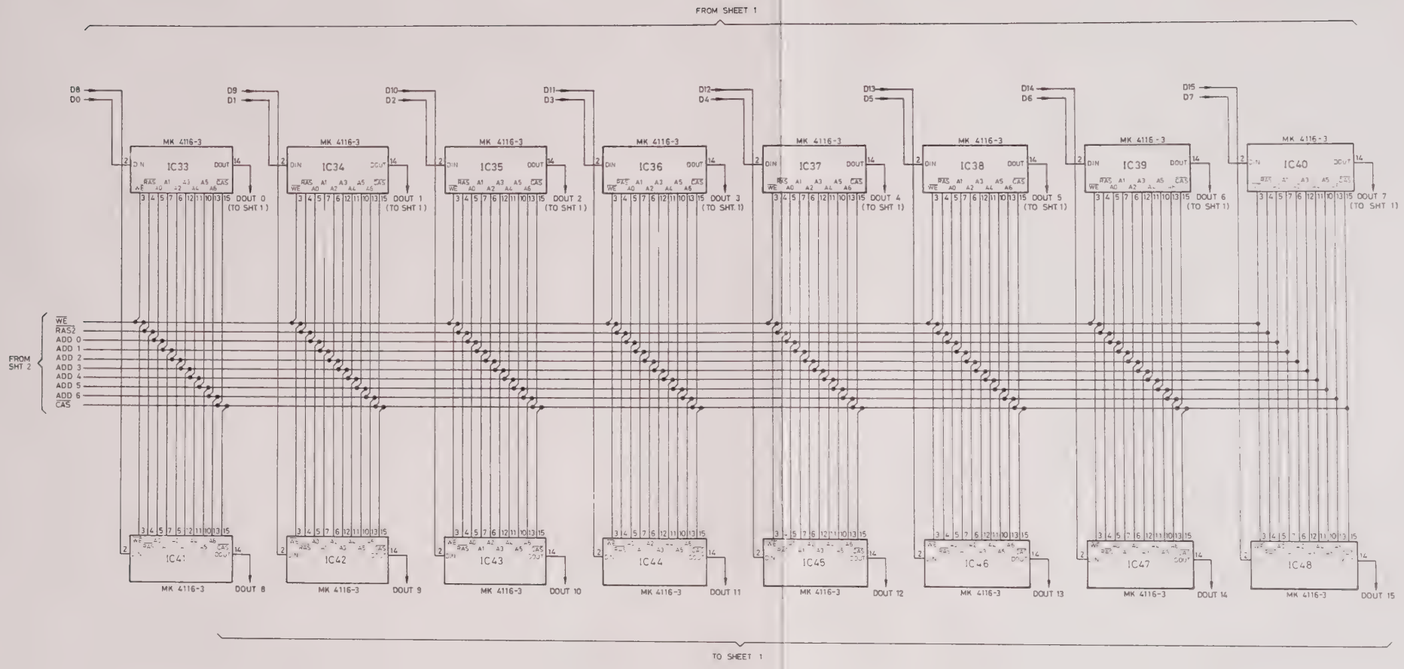
ARRAY PROCESSOR DIAGNOSTIC (3)
12007523 Issue C Sheet 3



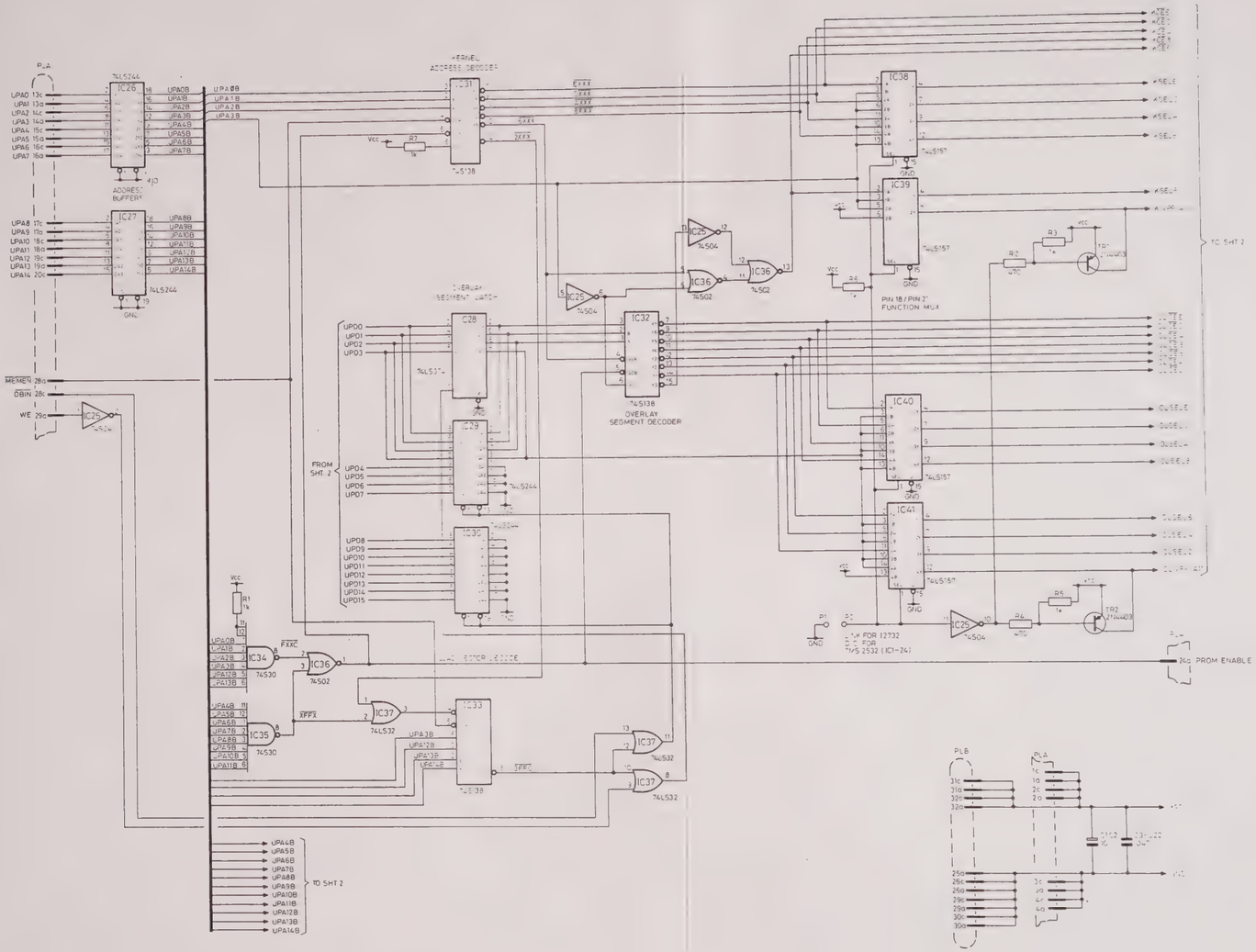
CONTROLLER STORE (1)
12007524 Issue B Sheet 1



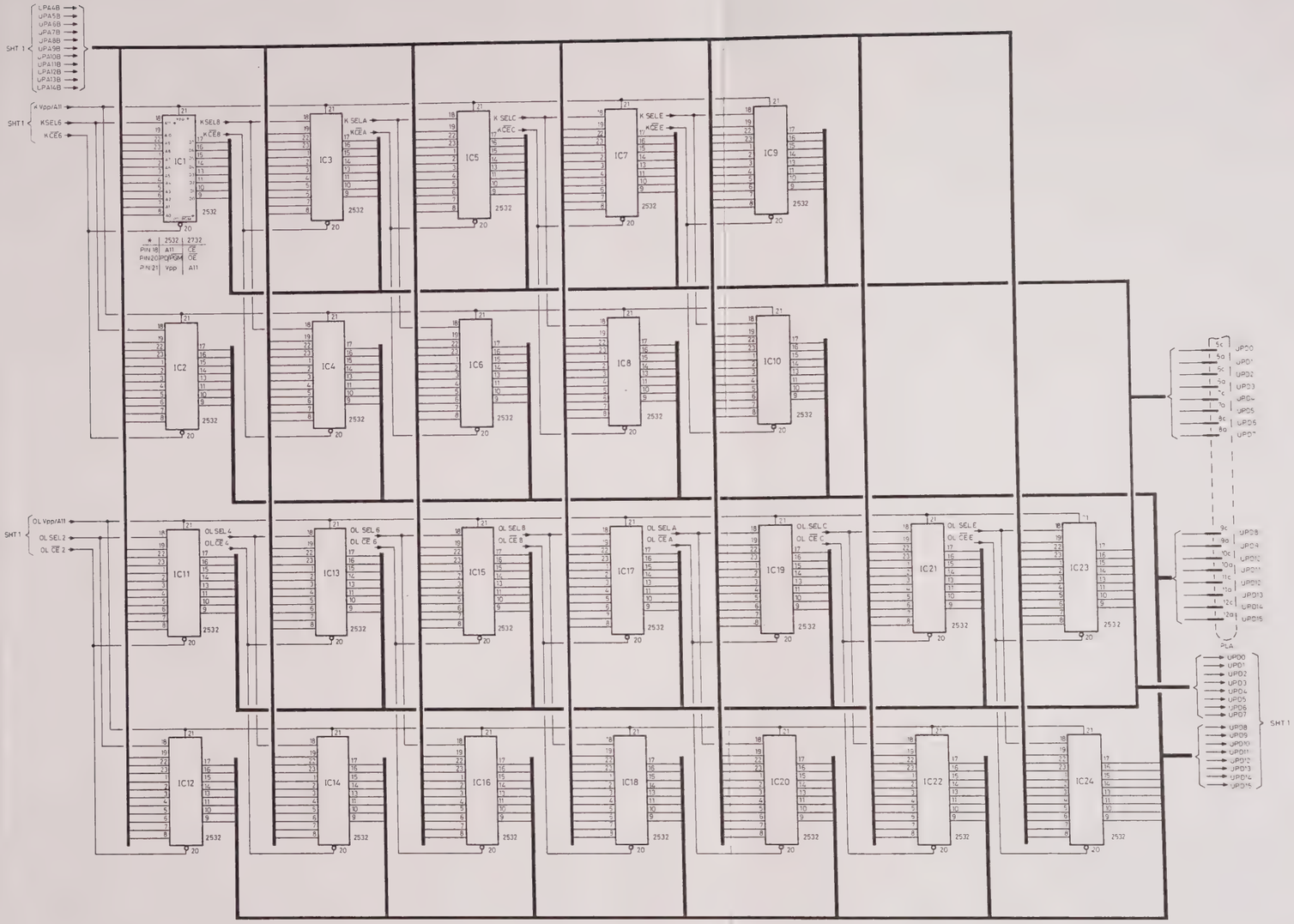
CONTROLLER STORE (2)
12007524 Issue B Sheet 2



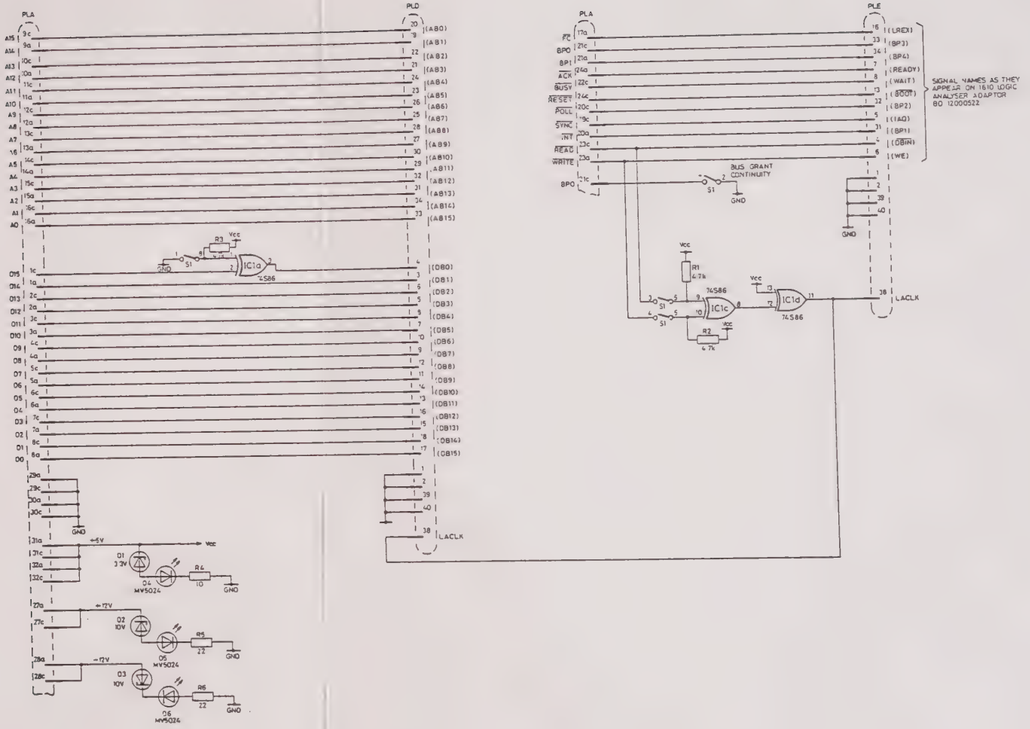
CONTROLLER STORE (3)
12007524 Issue B Sheet 3



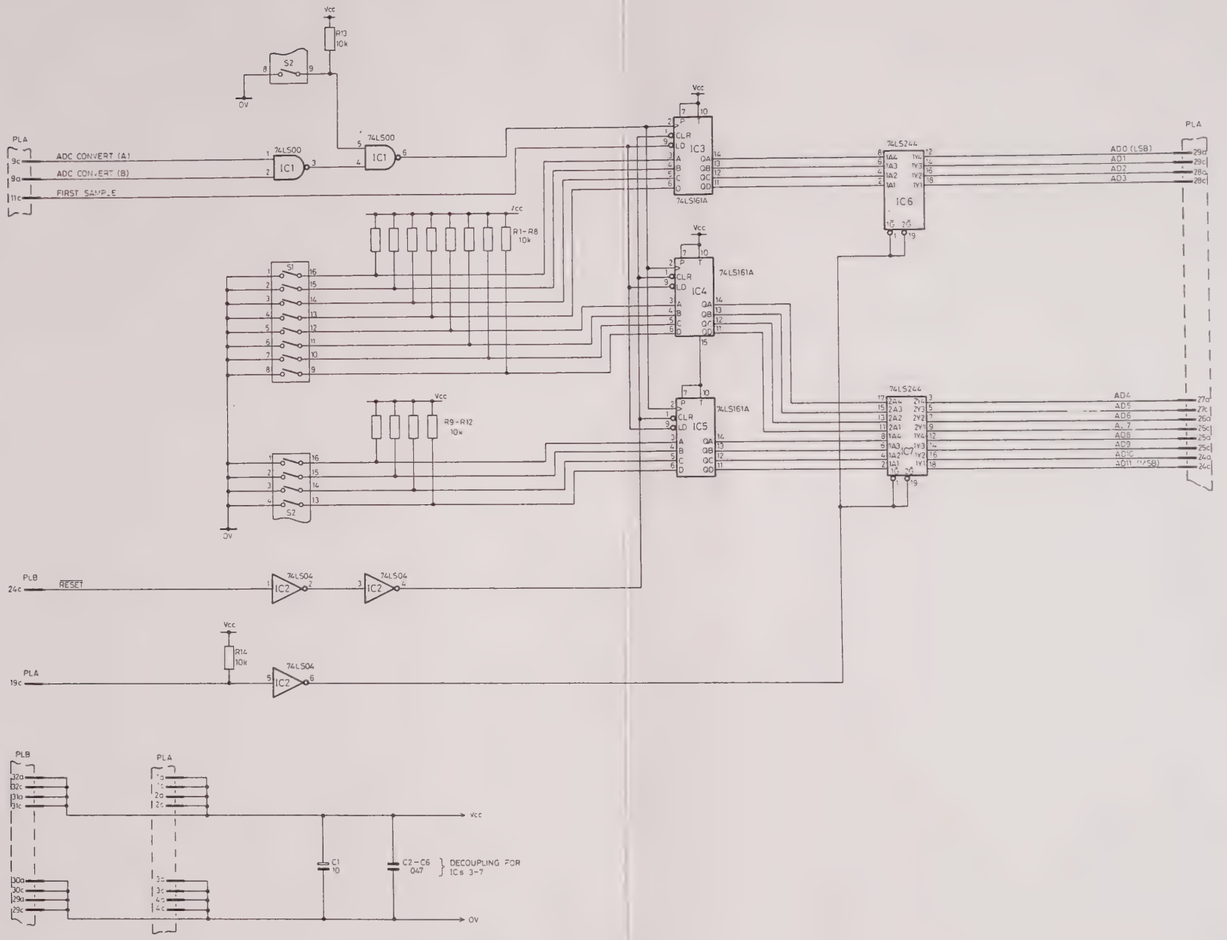
CONTROLLER INSTRUCTION STORE (1)
12007528 Issue B Sheet 1



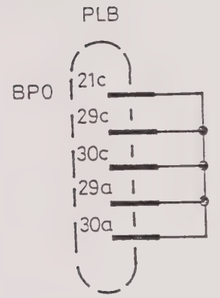
CONTROLLER INSTRUCTION STORE (2)
12007528 Issue B Sheet 2

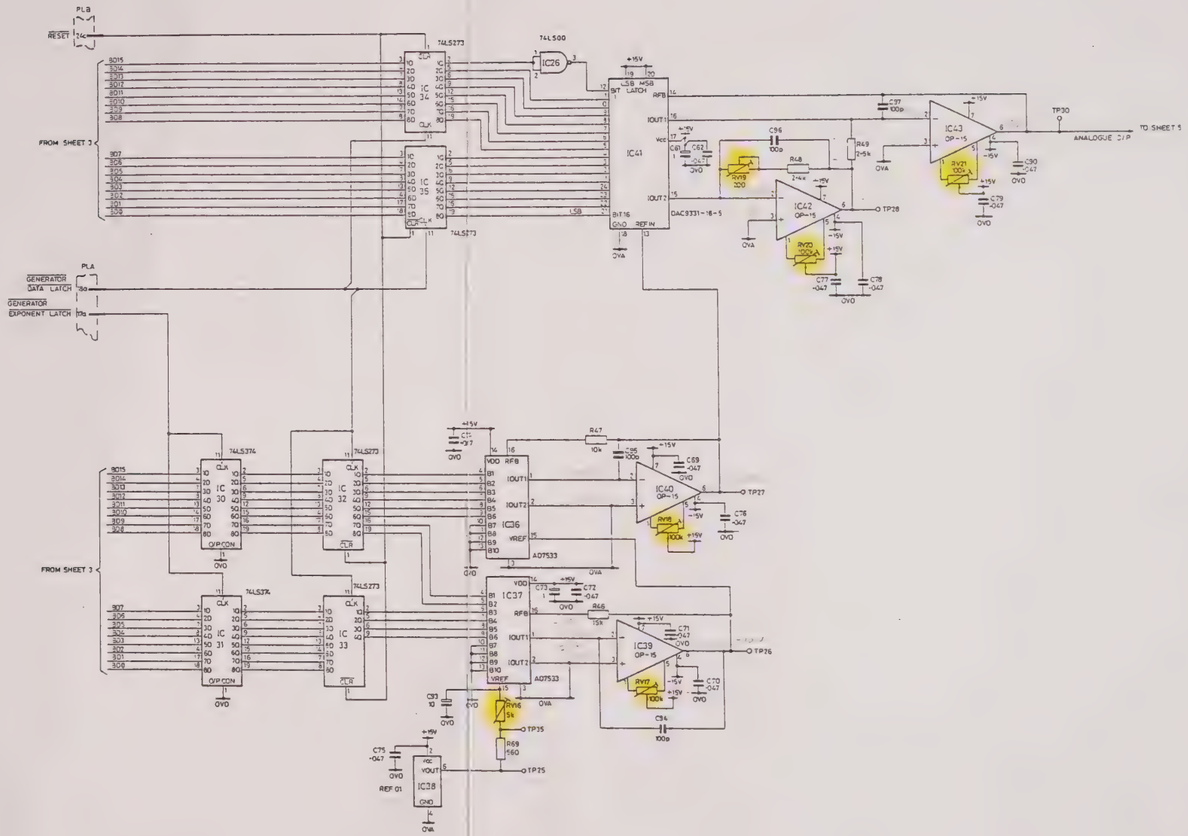


BUS LOGIC ANALYSER ADAPTOR
12007529 Issue C Sheet 1

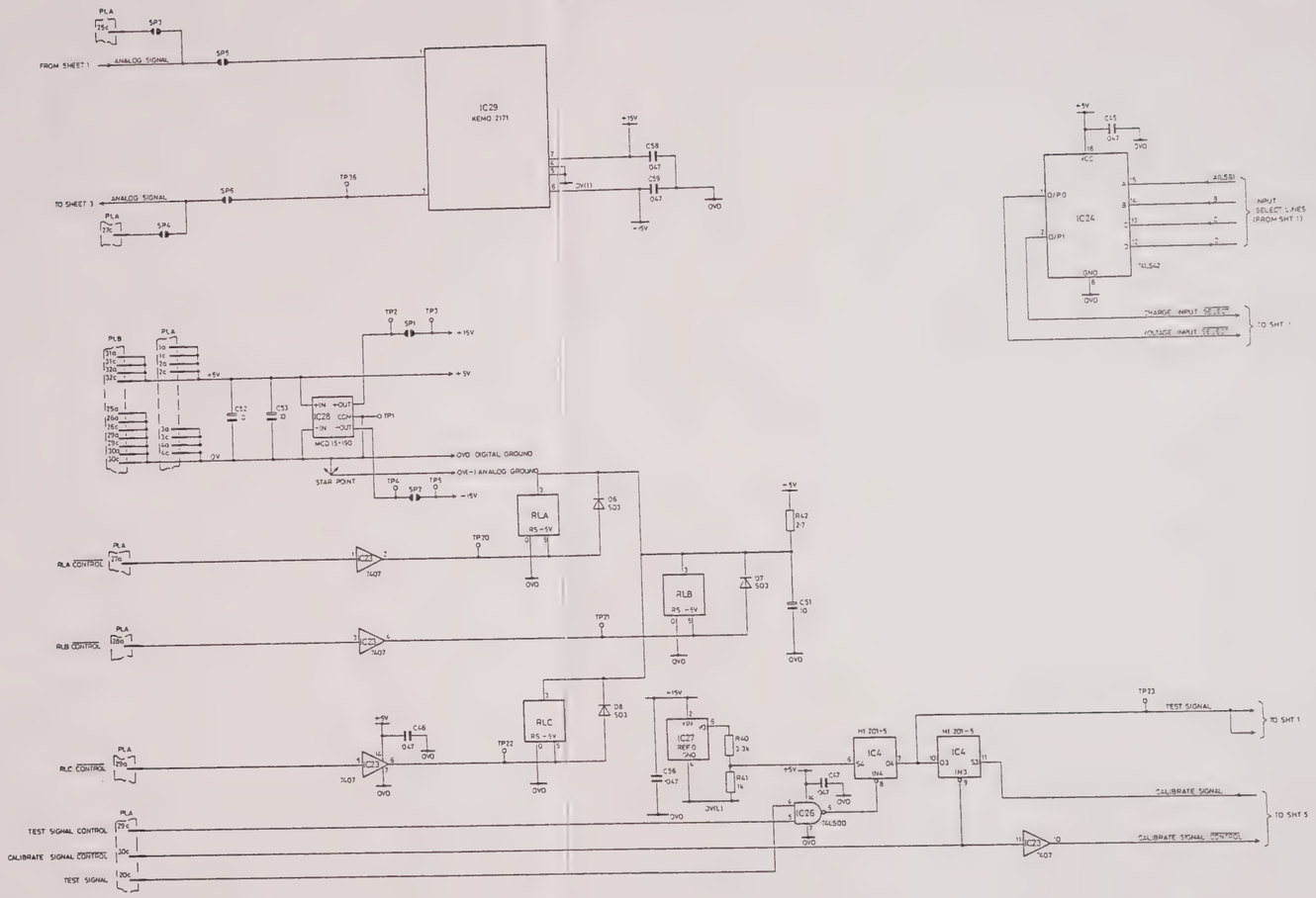


SIGNATURE ANALYSIS STIMULUS
12007531 Issue A Sheet 1

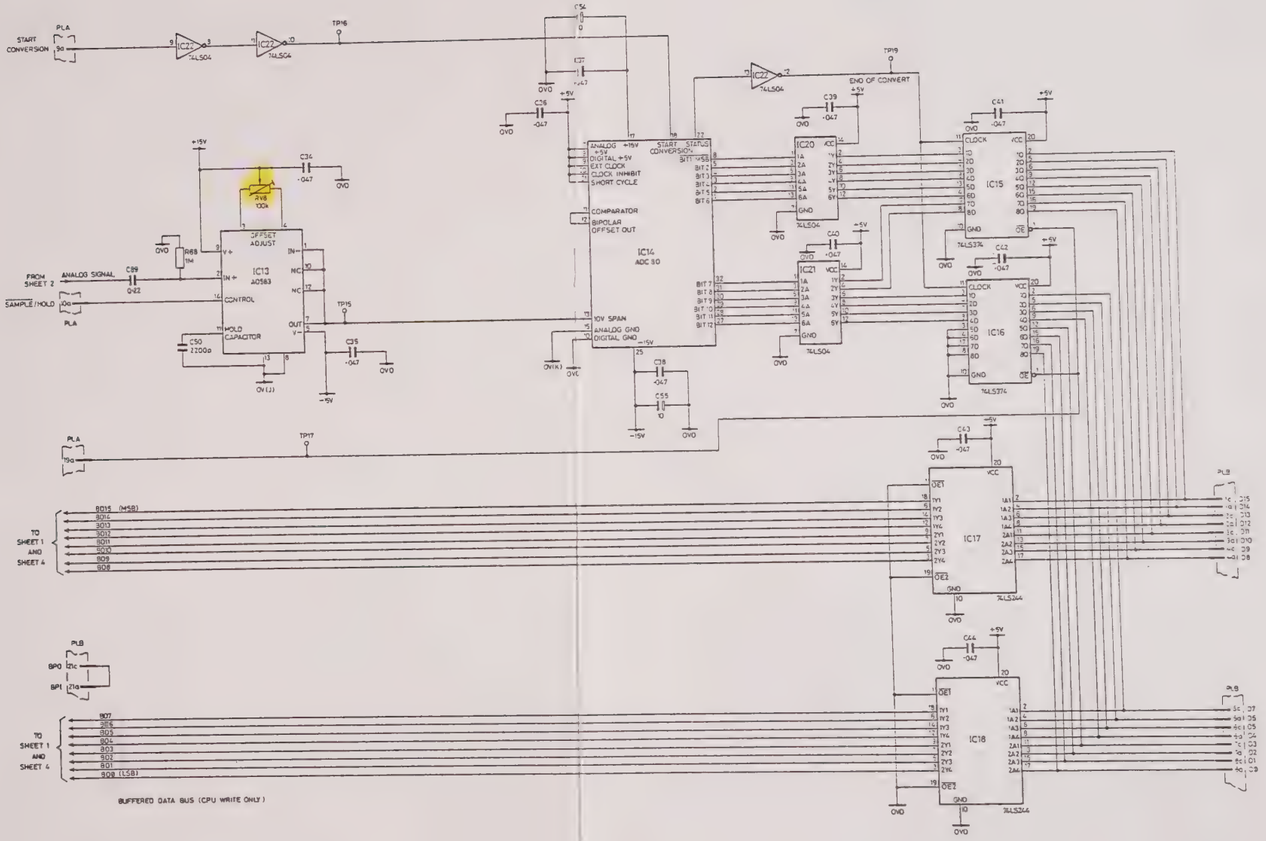

PLB
BP0
21c
29c
30c
29a
30a

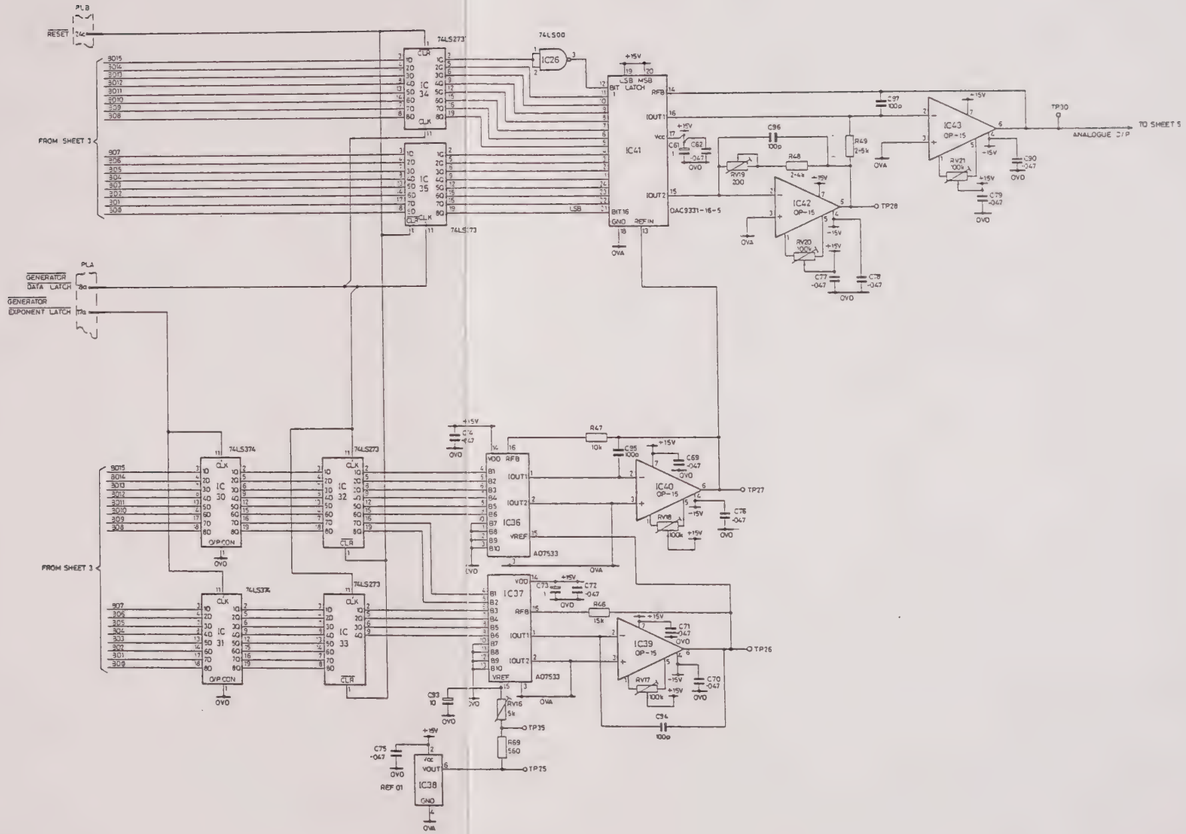


INPUT AND GENERATOR MODULE (4)
12007552 Issue F Sheet 4

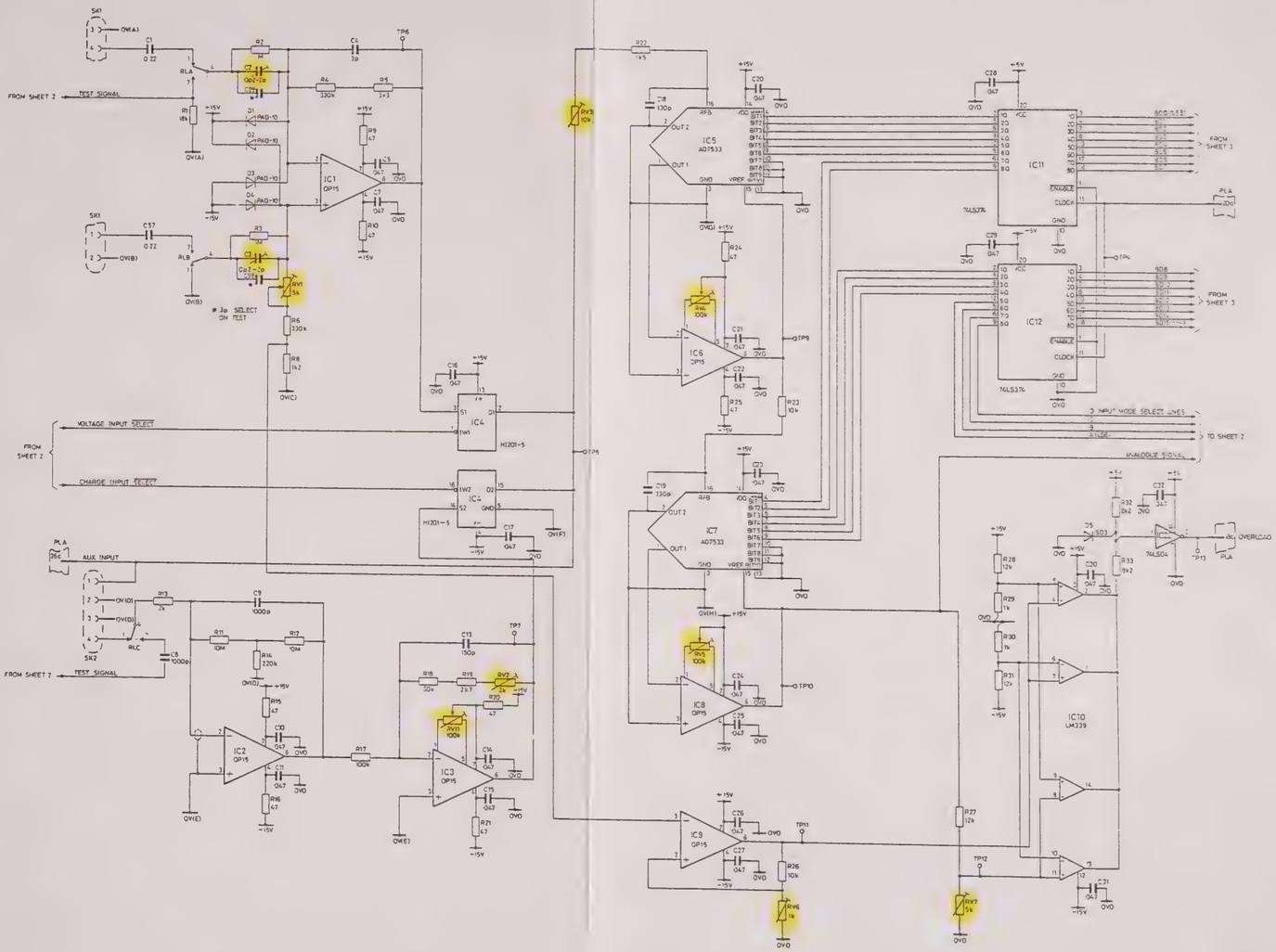


INPUT AND GENERATOR MODULE (2)
12007552 Issue F Sheet 2

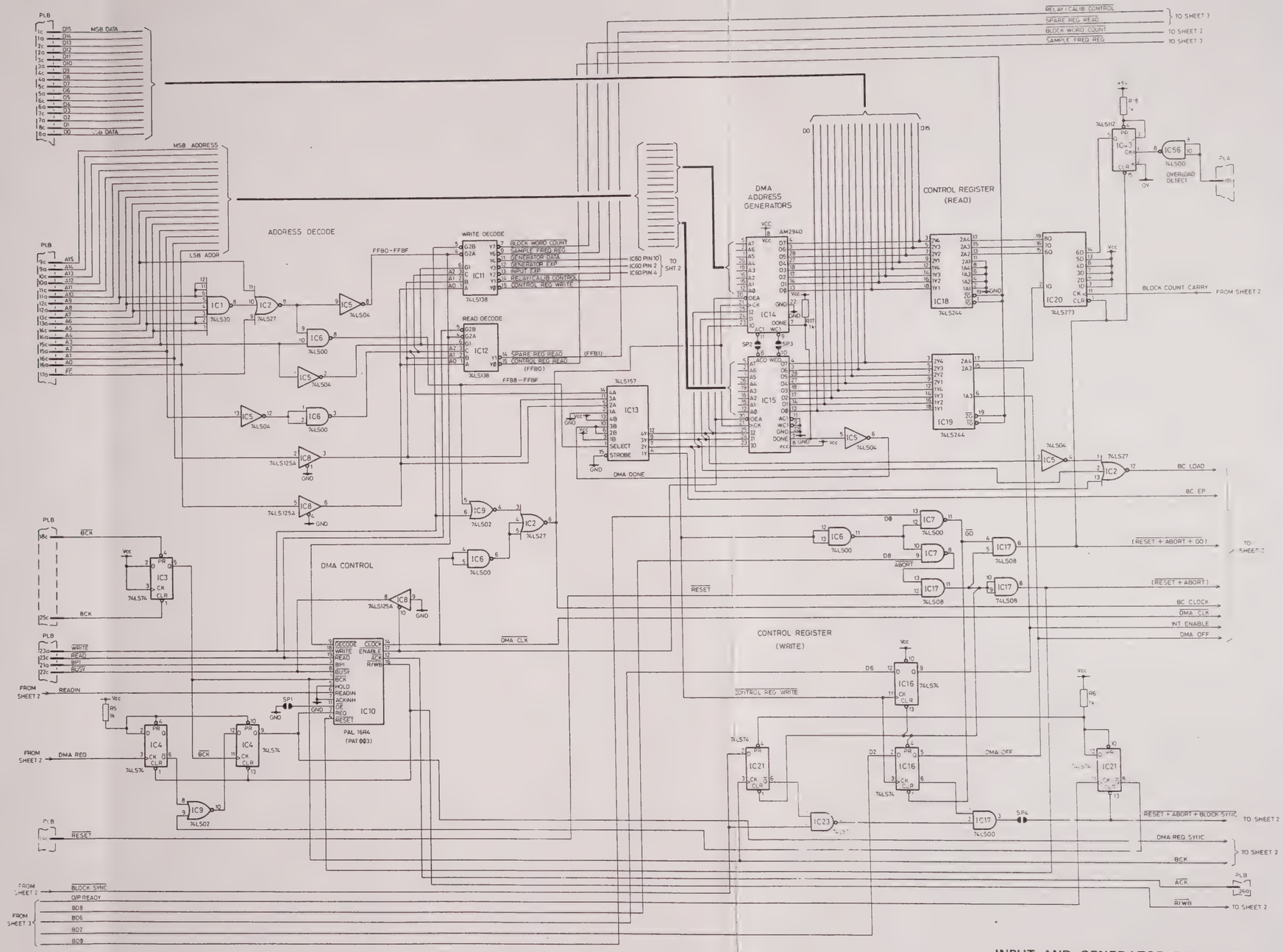

START CONVERSION
PL4
IC22
74LS04
TP16
C34
.047
+15V
0V8
100k
OFFSET ADJUST
R88
1M
FROM SHEET 2
ANALOG SIGNAL
C89
.022
SAMPLE/HOLD
PL4
IC13
AD583
CONTROL
HOLD CAPACITOR
C50
2200p
0V (2)
TP15
C35
.047
-15V
C54
0
C37
.047
C36
.047
ANALOG +15V
DIGITAL +5V
EXT CLOCK
CLOCK INHIBIT
SHORT CYCLE
COMPARATOR
BIPOLAR
OFFSET OUT
IC14
ADC 80
START CONVERSION
STATUS
BIT1
BIT2
BIT3
BIT4
BIT5
BIT6
BIT7
BIT8
BIT9
BIT10
BIT11
BIT12
10V SPAN
ANALOG GND
DIGITAL GND
0V(K)
0VL
C38
.047
C55
10
IC22
74LS04
TP19
END OF CONVERT
C39
.047
IC20
74LS04
C40
.047
IC21
74LS04
C41
.047
IC15
74LS374
C42
.047
IC16
74LS374
PL4
TP17
C43
.047
IC17
74LS244
PL8
BD15 (MSB)
BD14
BD13
BD12
BD11
BD10
BD9
BD8
TO SHEET 1 AND SHEET 4
PL8
BP0
BP1
C44
.047
IC18
74LS244
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0 (LSB)
TO SHEET 1 AND SHEET 4
BUFFERED DATA BUS (CPU WRITE ONLY)



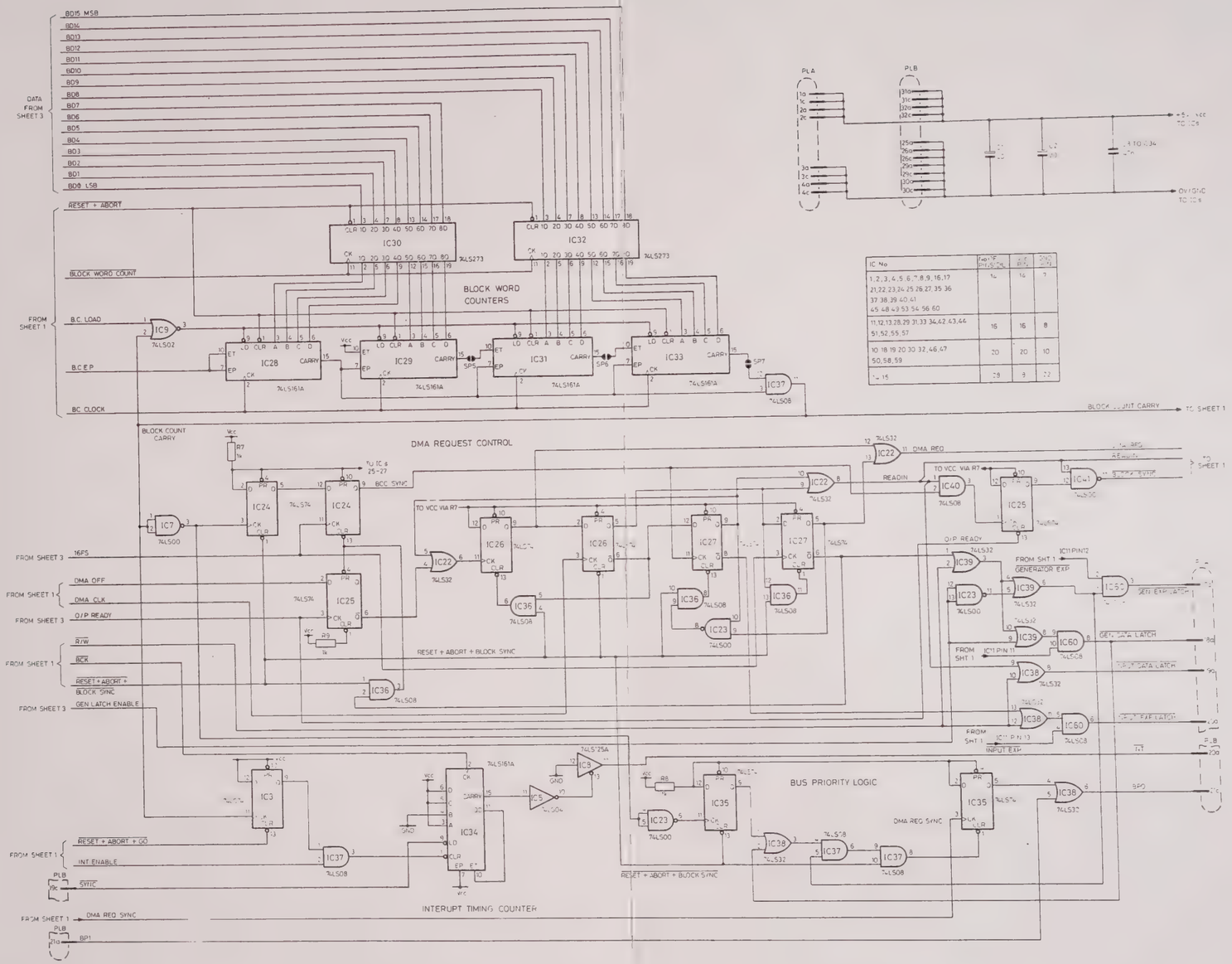
INPUT AND GENERATOR MODULE (4)
12007552 Issue F Sheet 4



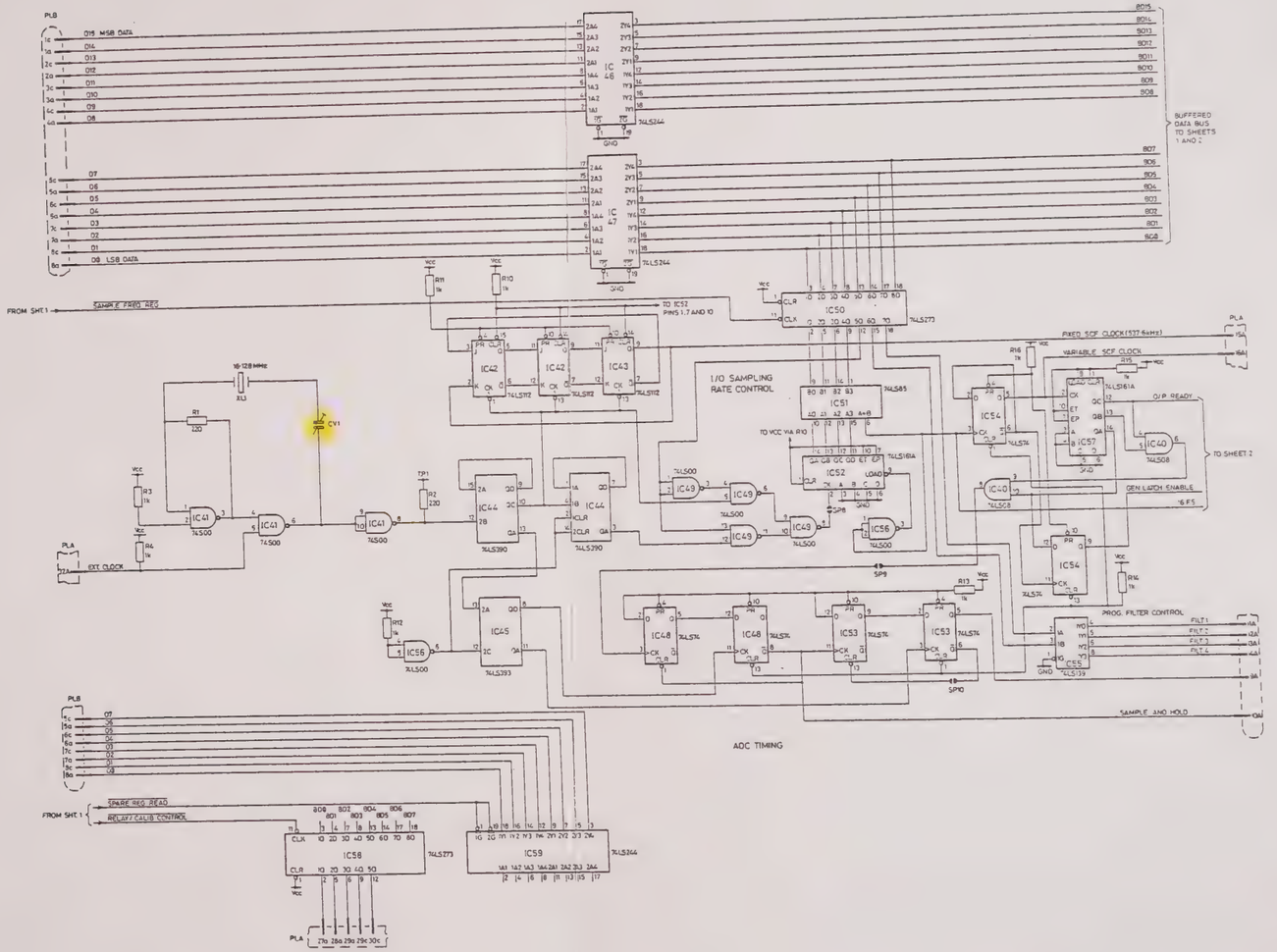
INPUT AND GENERATOR MODULE (1)
12007552 Issue G Sheet 1



INPUT AND GENERATOR DMA CONTROL (1)
12107551 Issue D Sheet 1

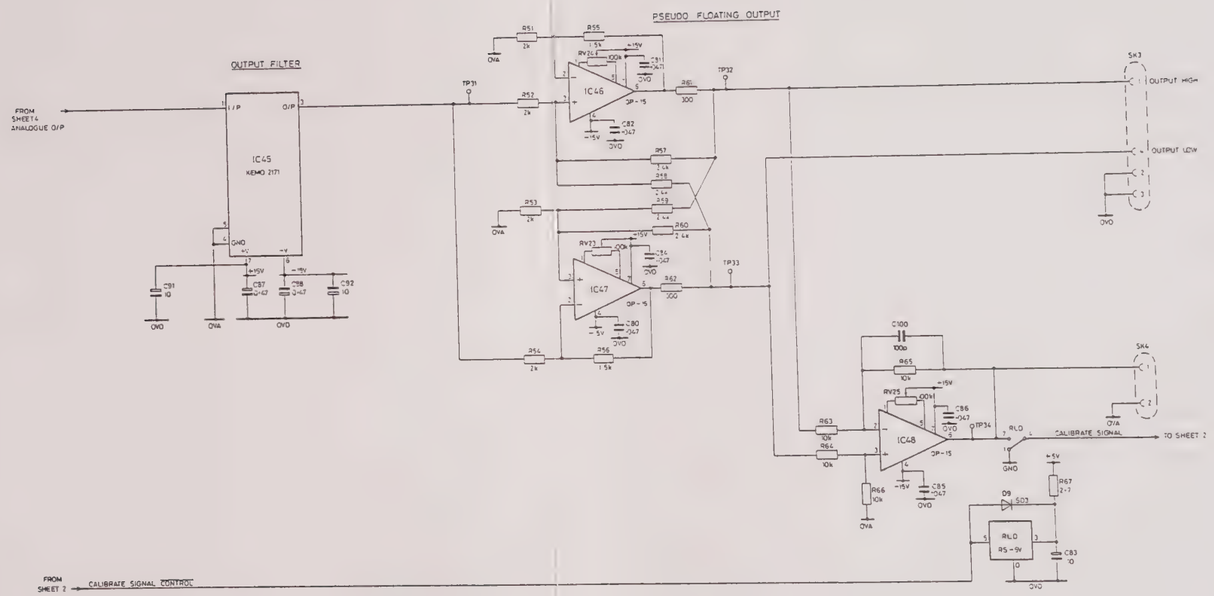


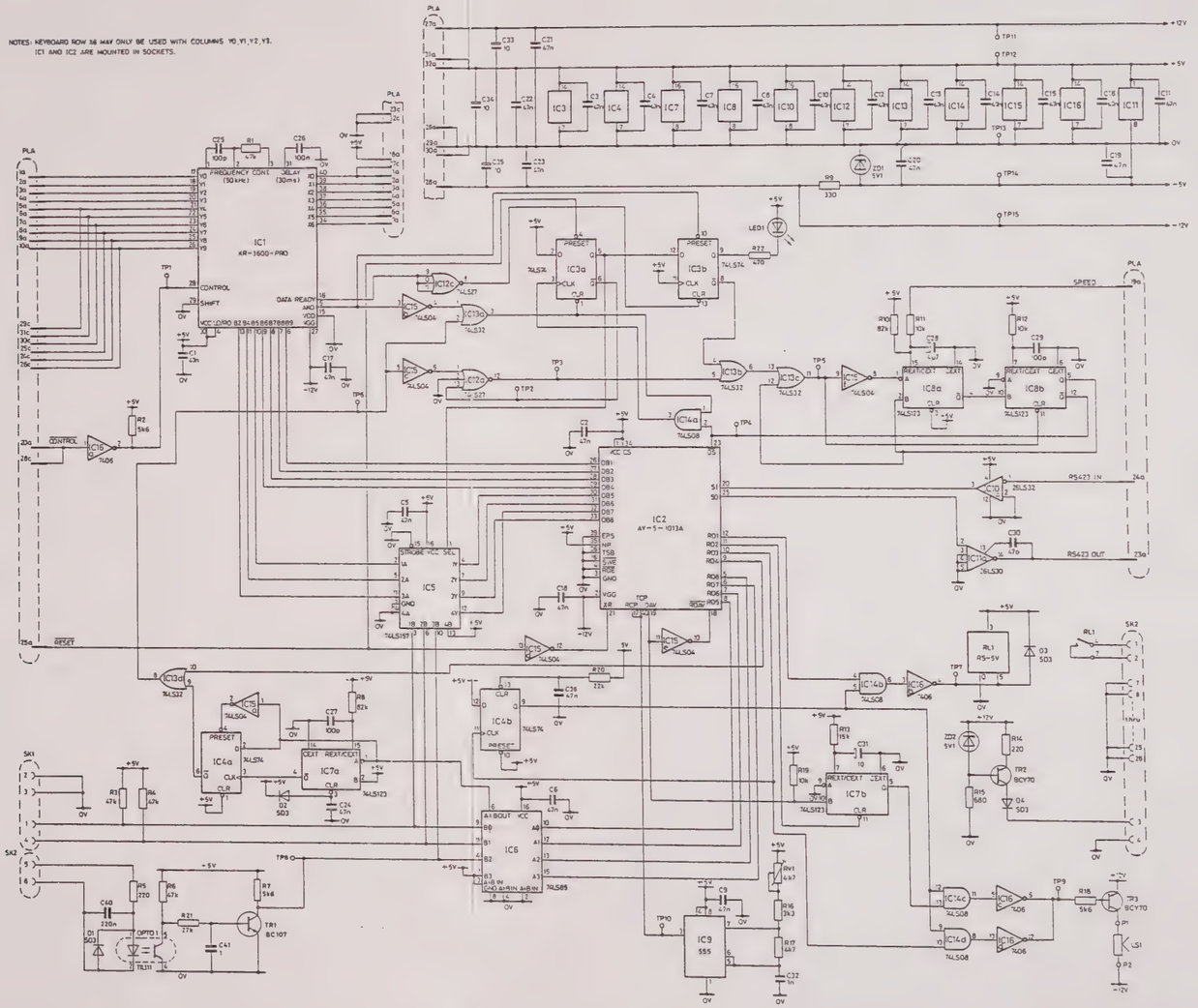
INPUT AND GENERATOR DMA CONTROL (2)
12107551 Issue D Sheet 2



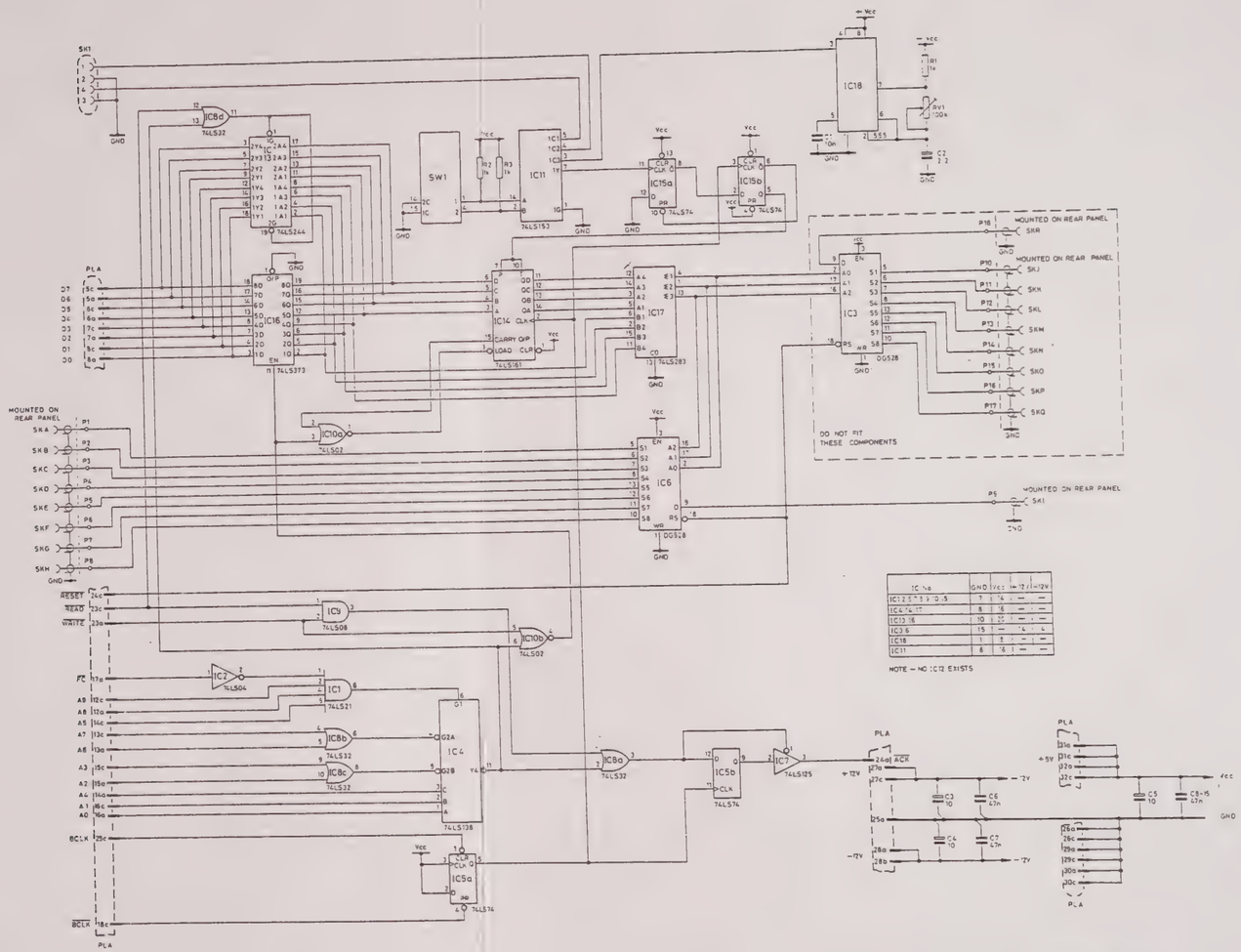
INPUT AND GENERATOR DMA CONTROL (3)

12007551 Issue E Sheet 3


OUTPUT FILTER
PSEUDO FLOATING OUTPUT
FROM SHEET 4 ANALOGUE O/P
I/P
O/P
IC45
KEMO 2171
GND
+V
-V
C91 10
C87 .047
C88 .047
C92 10
0VD
0VA
TP31
TP32
TP33
TP34
R51 2k
R52 2k
R53 2k
R54 2k
R55 5k
RV24 100k
C81 .047
IC46
DP-15
R61 100
C82 .047
+15V
-15V
R57 1k
R58 2k
R59 2k
R60 2.4k
RV23 100k
C84 .047
IC47
DP-5
R62 300
C80 .047
+5V
R56 1.5k
SK3
OUTPUT HIGH
OUTPUT LOW
C100 100p
R65 10k
RV25 100k
C86 .047
IC48
R63 10k
R64 10k
R66 10k
C85 .047
RL0
CALIBRATE SIGNAL
TO SHEET 2
SK4
D9 SD3
RL0 RS-5V
R67 2.7
C83 10
FROM SHEET 2
CALIBRATE SIGNAL CONTROL



KEYBOARD INTERFACE
12007553 Issue G Sheet 1

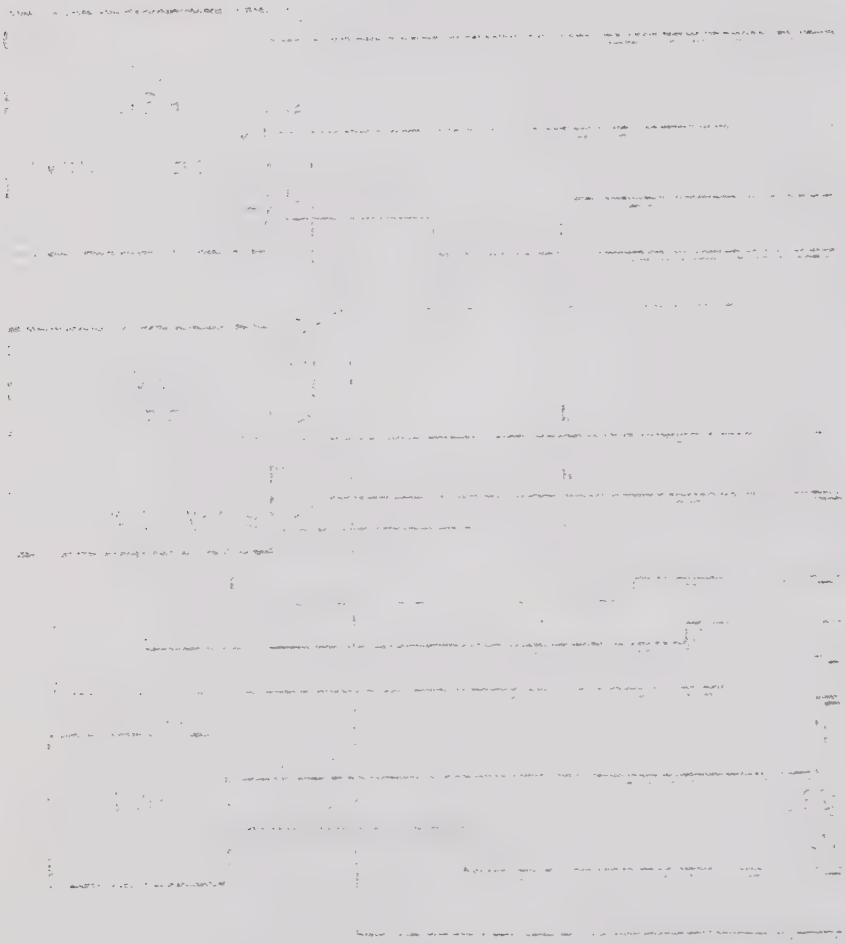


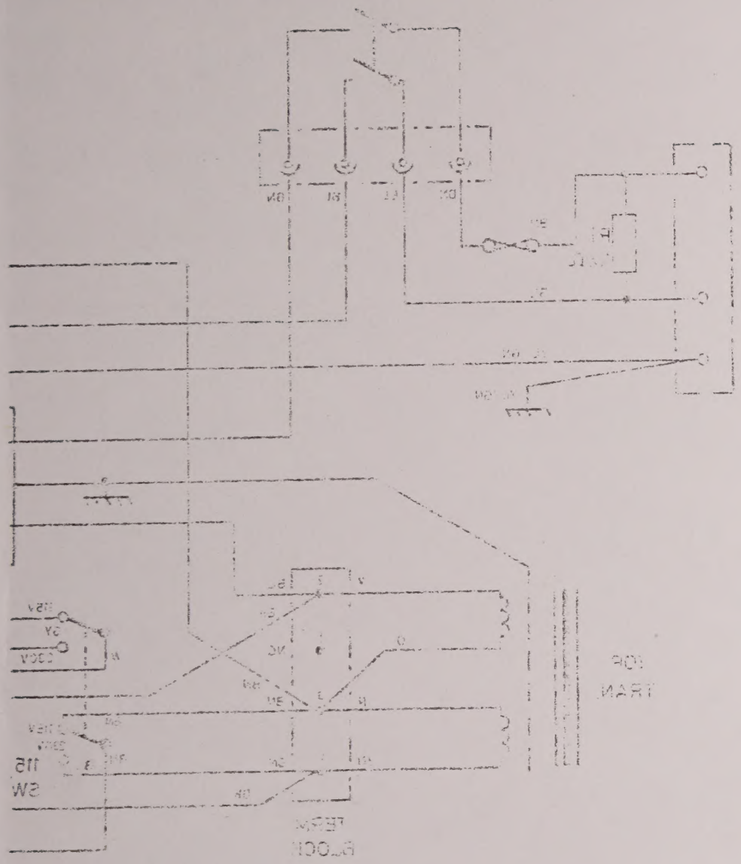
IC No	GND	Vcc	+12/+12V
IC1,2,3,5,9,10	7	14	—
IC4,14,17	8	16	—
IC13,16	10	20	—
IC15	15	—	4
IC18	1	8	—
IC11	8	16	—

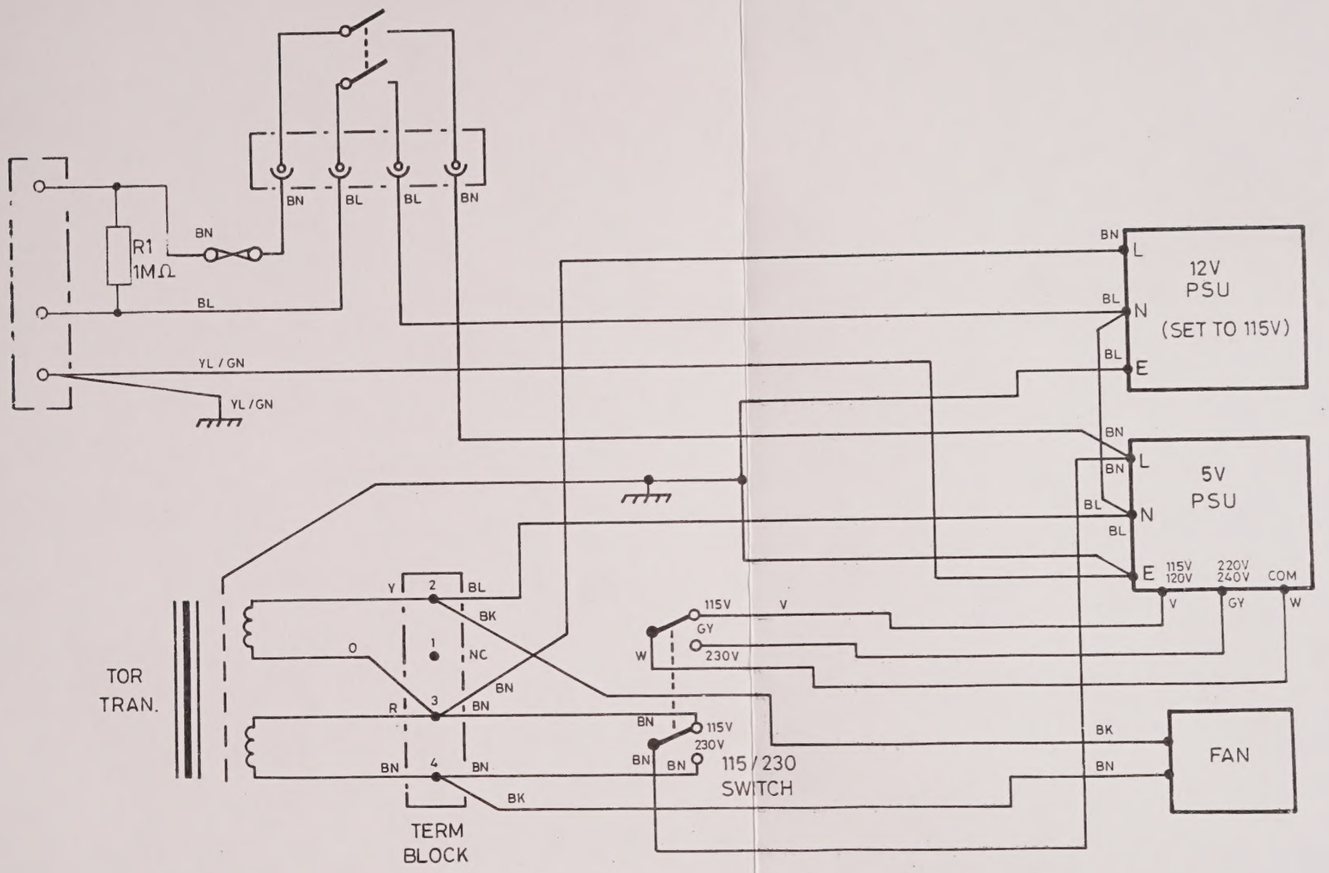
NOTE — NO IC12 EXISTS

SCANNER MODULE

12107555 Issue A , Sheet 1.







AC SUPPLY CIRCUIT
12007002 Issue C Sheet 1